

PCF85063BTL

Tiny Real-Time Clock/calendar with alarm function and SPI-bus

Rev. 2 — 15 April 2013

Product data sheet

1. General description

The PCF85063BTL is a CMOS¹ Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.25 Mbit/s. The register address is incremented automatically after each written or read data byte.

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 0.9 V to 5.5 V
- Low current; typical 0.22 μ A at $V_{DD} = 3.3$ V and $T_{amb} = 25$ °C
- 3 line SPI-bus with a maximum data rate of 7 Mbit/s
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Selectable integrated oscillator load capacitors for $C_L = 7$ pF or $C_L = 12.5$ pF
- Alarm function
- Countdown timer
- Minute and half minute interrupt
- Internal Power-On Reset (POR)
- Programmable offset register for frequency adjustment

3. Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 19](#).



4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|--|-----------|
| | Name | Description | Version |
| PCF85063BTL | HXSON10 | plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 × 2.6 × 0.5 mm | SOT1197-1 |

4.1 Ordering options

Table 2. Ordering options

| Product type number | IC revision | Sales item (12NC) | Delivery form |
|---------------------|-------------|-------------------|------------------------|
| PCF85063BTL/1 | 1 | 935299022118 | tape and reel, 13 inch |

5. Marking

Table 3. Marking codes

| Product type number | Marking code |
|---------------------|--------------|
| PCF85063BTL | 063B |

6. Block diagram

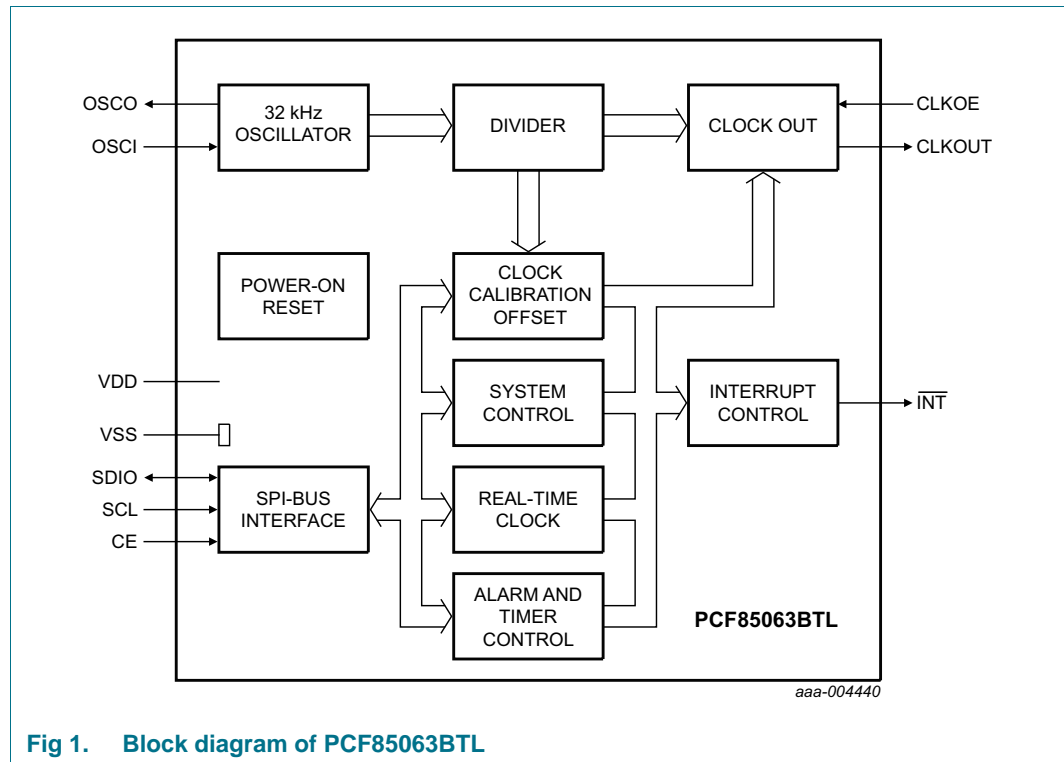
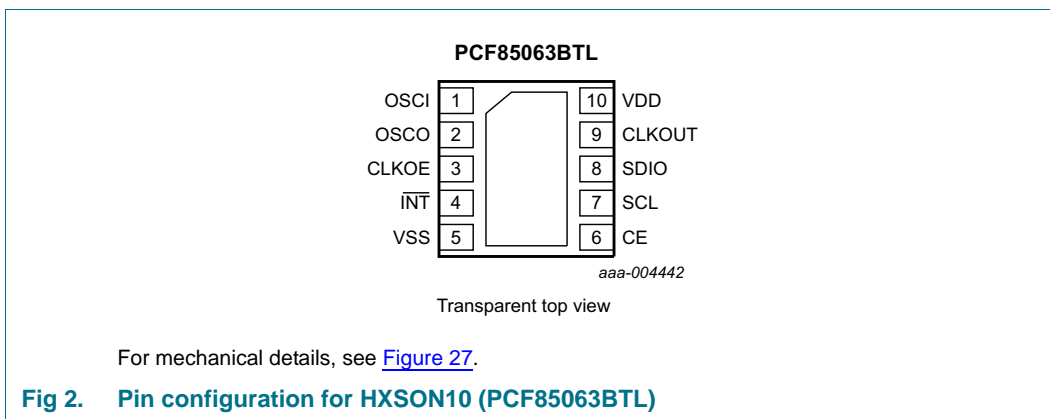


Fig 1. Block diagram of PCF85063BTL

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4. Pin description

| Symbol | Pin | Type | Description |
|--------|------------------|--------------|---|
| OSCI | 1 | input | oscillator input |
| OSCO | 2 | output | oscillator output |
| CLKOE | 3 | input | CLKOUT enable or disable pin; enable is active HIGH |
| INT | 4 | output | interrupt output (open-drain) |
| VSS | 5 ^[1] | supply | ground supply voltage |
| CE | 6 | input | chip enable |
| SCL | 7 | input | serial clock input |
| SDIO | 8 | input/output | serial data input and output |
| CLKOUT | 9 | output | clock output (push-pull) |
| VDD | 10 | supply | supply voltage |

[1] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

8. Functional description

The PCF85063BTL contains 18 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calendar, and SPI-bus with a maximum data rate of 6.25 Mbit/s.

The built-in address register will increment automatically after each read or write of a data byte up to the register 11h. After register 11h, the auto-incrementing will wrap around to address 00h (see [Figure 3](#)).

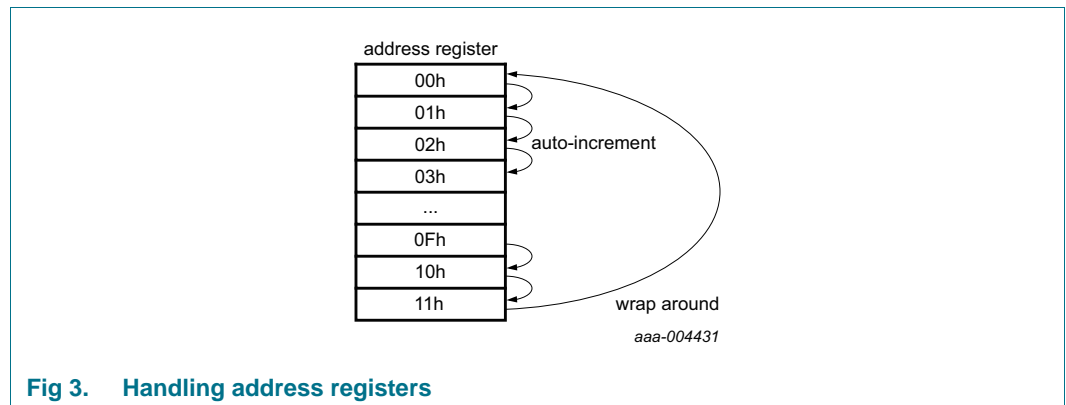


Fig 3. Handling address registers

All registers (see [Table 5](#)) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and status register. The register at address 02h is an offset register allowing the fine-tuning of the clock; and at 03h is a free RAM byte. The addresses 04h through 0Ah are used as counters for the clock function (seconds up to years counters). Address locations 0Bh through 0Fh contain alarm registers which define the conditions for an alarm. The registers at 10h and 11h are for the timer function.

The Seconds, Minutes, Hours, Days, Months, and Years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

8.1 Registers organization

Table 5. Registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to [Table 8 on page 9](#).

| Address | Register name | Bit | | | | | | | | Reference | |
|-------------------------------------|---------------|-----------------|------------------------|--------------------------------------|--------------------------------------|----|------------------------|-------|---------|-------------------------------|-------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Control and status registers | | | | | | | | | | | |
| 00h | Control_1 | EXT_TEST | - | STOP | SR | - | CIE | 12_24 | CAP_SEL | Section 8.2.1 | |
| 01h | Control_2 | AIE | AF | MI | HMI | TF | COF[2:0] | | | Section 8.2.2 | |
| 02h | Offset | MODE | OFFSET[6:0] | | | | | | | | Section 8.2.3 |
| 03h | RAM_byte | B[7:0] | | | | | | | | | Section 8.2.4 |
| Time and date registers | | | | | | | | | | | |
| 04h | Seconds | OS | SECONDS (0 to 59) | | | | | | | | Section 8.3.1 |
| 05h | Minutes | - | MINUTES (0 to 59) | | | | | | | | Section 8.3.2 |
| 06h | Hours | - | - | AMPM | HOURS (1 to 12) in 12 hour mode | | | | | | Section 8.3.3 |
| | | | | HOURS (0 to 23) in 24 hour mode | | | | | | | |
| 07h | Days | - | - | DAYS (1 to 31) | | | | | | | Section 8.3.4 |
| 08h | Weekdays | - | - | - | - | - | WEEKDAYS (0 to 6) | | | | Section 8.3.5 |
| 09h | Months | - | - | - | MONTHS (1 to 12) | | | | | | Section 8.3.6 |
| 0Ah | Years | YEARS (0 to 99) | | | | | | | | | Section 8.3.7 |
| Alarm registers | | | | | | | | | | | |
| 0Bh | Second_alarm | AEN_S | SECOND_ALARM (0 to 59) | | | | | | | | Section 8.5.1 |
| 0Ch | Minute_alarm | AEN_M | MINUTE_ALARM (0 to 59) | | | | | | | | Section 8.5.2 |
| 0Dh | Hour_alarm | AEN_H | - | AMPM | HOUR_ALARM (1 to 12) in 12 hour mode | | | | | | Section 8.5.3 |
| | | | | HOUR_ALARM (0 to 23) in 24 hour mode | | | | | | | |
| 0Eh | Day_alarm | AEN_D | - | DAY_ALARM (1 to 31) | | | | | | | Section 8.5.4 |
| 0Fh | Weekday_alarm | AEN_W | - | - | - | - | WEEKDAY_ALARM (0 to 6) | | | | Section 8.5.5 |
| Timer registers | | | | | | | | | | | |
| 10h | Timer_value | T[7:0] | | | | | | | | | Section 8.6.1 |
| 11h | Timer_mode | - | - | - | TCF[1:0] | TE | TIE | TI_TP | | | Section 8.6.2 |

8.2 Control registers

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

| Bit | Symbol | Value | Description | Reference |
|-----|----------|------------------|--|--|
| 7 | EXT_TEST | | external clock test mode | Section 8.2.1.1 |
| | | 0 ^[1] | normal mode | |
| | | 1 | external clock test mode | |
| 6 | - | 0 | unused | - |
| 5 | STOP | | STOP bit | Section 8.2.1.2 |
| | | 0 ^[1] | RTC clock runs | |
| | | 1 | RTC clock is stopped; all RTC divider chain flip-flops are asynchronously set logic 0 | |
| 4 | SR | | software reset | Section 8.2.1.3 |
| | | 0 ^[1] | no software reset | |
| | | 1 | initiate software reset ^[2] ; this bit always returns a 0 when read | |
| 3 | - | 0 | unused | - |
| 2 | CIE | | correction interrupt enable | Section 8.2.3 |
| | | 0 ^[1] | no correction interrupt generated | |
| | | 1 | interrupt pulses are generated at every correction cycle | |
| 1 | 12_24 | | 12 or 24 hour mode | Section 8.3.3 Section 8.5.3 |
| | | 0 ^[1] | 24 hour mode is selected | |
| | | 1 | 12 hour mode is selected | |
| 0 | CAP_SEL | | internal oscillator capacitor selection for quartz crystals with a corresponding load capacitance | - |
| | | 0 ^[1] | 7 pF | |
| | | 1 | 12.5 pF | |

[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see [Section 8.2.1.3](#)).

8.2.1.1 EXT_TEST: external clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2⁶ divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.2.1.2 STOP: STOP bit function

The function of the STOP bit (see [Figure 4](#)) is to allow for accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F₂ to F₁₄) to be held in reset and thus no 1 Hz ticks are generated. It also stops the output of clock frequencies lower than 8 kHz on pin CLKOUT.

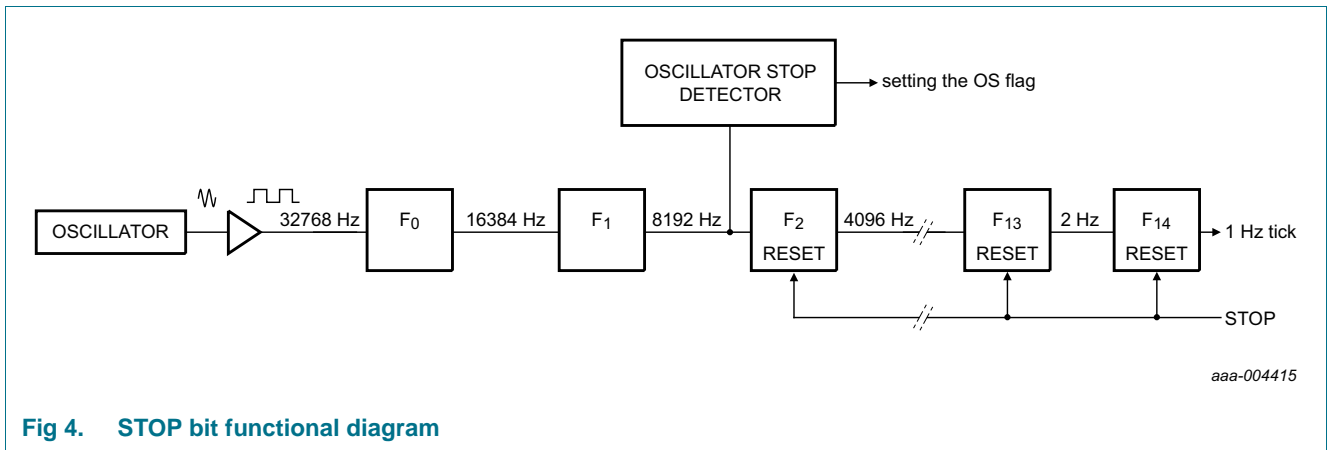
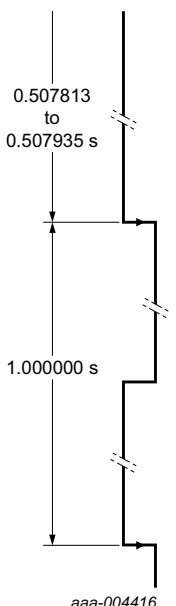


Fig 4. STOP bit functional diagram

The time circuits can then be set and do not increment until the STOP bit is released (see [Figure 5](#) and [Table 7](#)).

Table 7. First increment of time circuits after STOP bit release

| Bit | Prescaler bits ^[1] | 1 Hz tick | Time | Comment |
|--|--|-----------|----------|---|
| STOP | F ₀ F ₁ -F ₂ to F ₁₄ | | hh:mm:ss | |
| Clock is running normally | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | prescaler counting normally |
| STOP bit is activated by user. F₀F₁ are not reset and values cannot be predicted externally | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | prescaler is reset; time circuits are frozen |
| New time is set by user | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is reset; time circuits are frozen |
| STOP bit is released by user | | | | |
| 0 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of F ₁₄ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of F ₁₄ increments the time circuits |



[1] F₀ is clocked at 32.768 kHz.

The lower two stages of the prescaler (F₀ and F₁) are not reset. And because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see Figure 5).

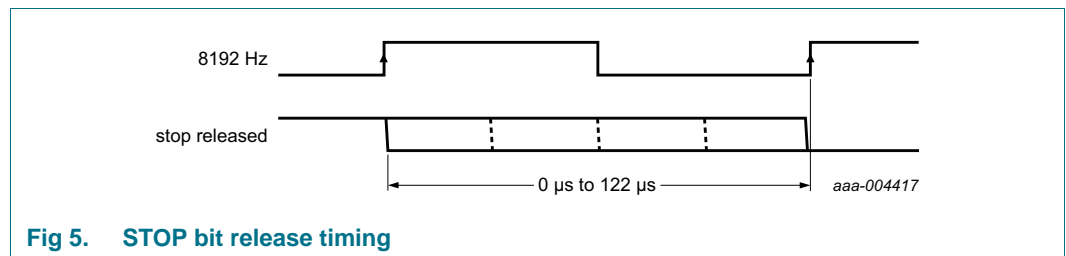


Fig 5. STOP bit release timing

The first increment of the time circuits is between 0.507 813 s and 0.507 935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F₀ and F₁ not being reset (see Table 7) and the unknown state of the 32 kHz clock.

8.2.1.3 Software reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see [Figure 6](#).

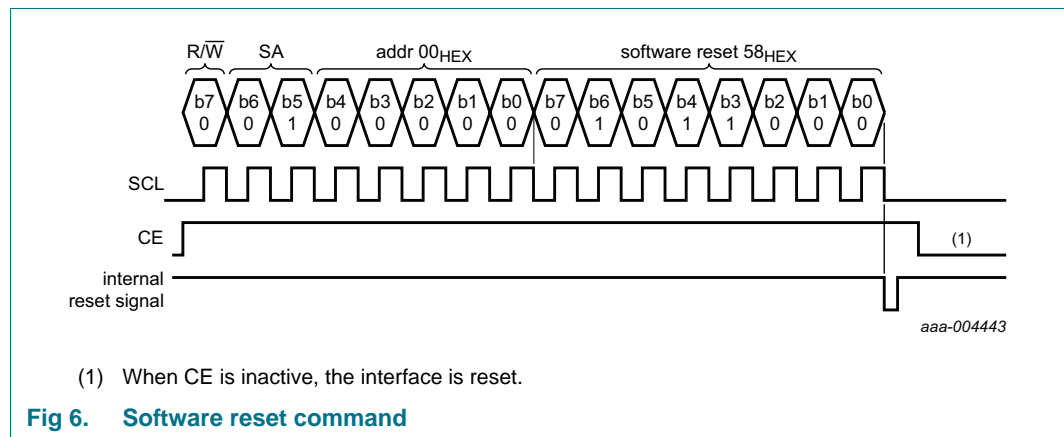


Fig 6. Software reset command

In reset state all registers are set according to [Table 8](#) and the address pointer returns to address 00h.

Table 8. Registers reset values

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Control_1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | Control_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Offset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | RAM_byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | Seconds | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | Minutes | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | Hours | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | Days | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 08h | Weekdays | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 09h | Months | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0Ah | Years | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | Second_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | Minute_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | Hour_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Day_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Fh | Weekday_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | Timer_value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | Timer_mode | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

The PCF85063BTL resets to:

Time — 00:00:00

Date — 20000101

Weekday — Saturday

8.2.2 Register Control_2

Table 9. Control_2 - control and status register 2 (address 01h) bit description

| Bit | Symbol | Value | Description | Reference |
|--------|----------|------------------------------|--|---|
| 7 | AIE | | alarm interrupt | Section 8.2.2.1 Section 8.5.6 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 6 | AF | | alarm flag | Section 8.2.2.1 Section 8.5.6 |
| | | 0 ^[1] | read: alarm flag inactive write: alarm flag is cleared | |
| | | 1 | read: alarm flag active write: alarm flag remains unchanged | |
| 5 | MI | | minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 4 | HMI | | half minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0 ^[1] | disabled | |
| | | 1 | enabled | |
| 3 | TF | | timer flag | Section 8.2.2.1 Section 8.2.2.3 Section 8.6.3 |
| | | 0 ^[1] | no timer interrupt generated | |
| | | 1 | flag set when timer interrupt generated | |
| 2 to 0 | COF[2:0] | see Table 11 | CLKOUT control | Section 8.2.2.4 |

[1] Default value.

8.2.2.1 Alarm interrupt

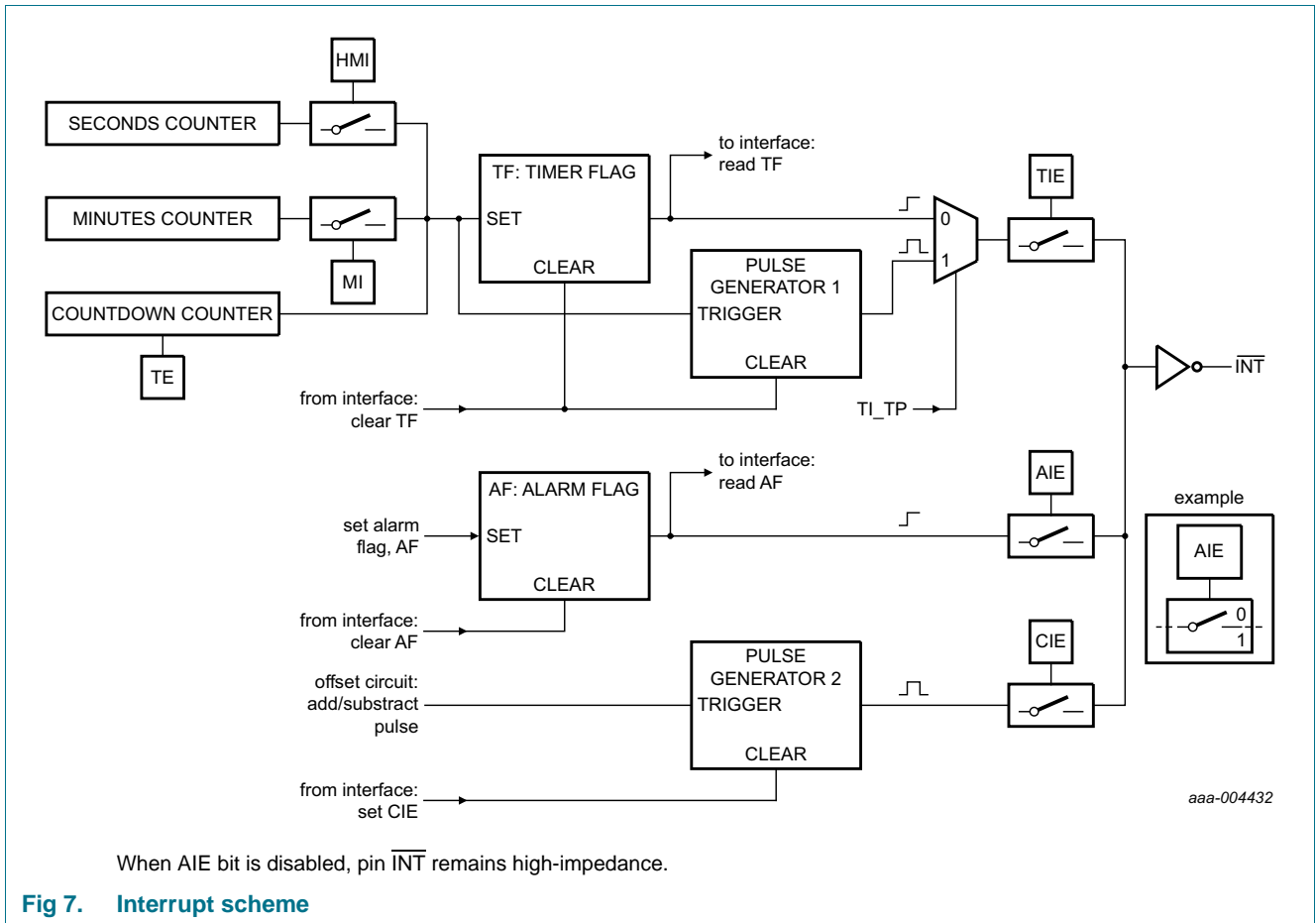


Fig 7. Interrupt scheme

AIE: This bit activates or deactivates the generation of an interrupt when AF is asserted, respectively.

AF: When an alarm occurs, AF is set logic 1. This bit maintains its value until overwritten by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

8.2.2.2 MI and HMI: minute and half minute interrupt

The minute interrupt (bit MI) and half minute interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin INT; see Figure 8. The timers are running in sync with the seconds counter (see Table 19 on page 18).

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds. Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a half minute interrupt is not distinguishable.

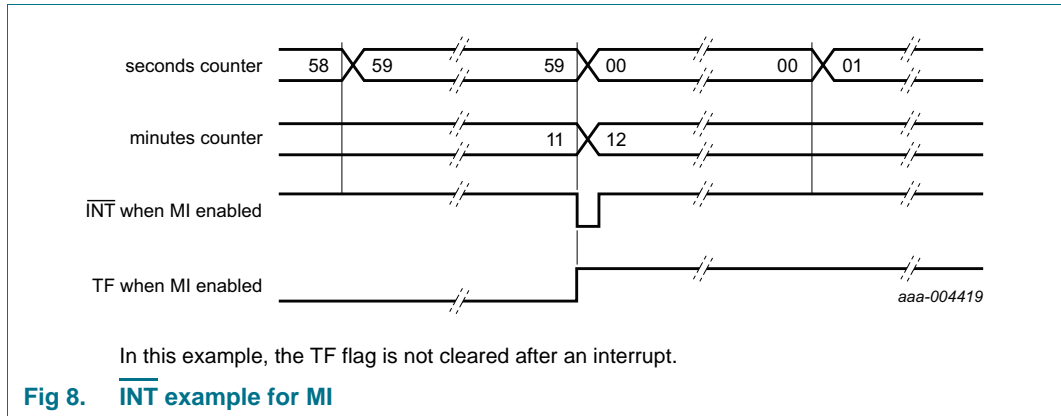


Table 10. Effect of bits MI and HMI on $\overline{\text{INT}}$ generation

| Minute interrupt (bit MI) | Half minute interrupt (bit HMI) | Result |
|---------------------------|---------------------------------|---------------------------|
| 0 | 0 | no interrupt generated |
| 1 | 0 | an interrupt every minute |
| 0 | 1 | an interrupt every 30 s |
| 1 | 1 | an interrupt every 30 s |

The duration of the timer is affected by the register Offset (see [Section 8.2.3](#)). Only when OFFSET[6:0] has the value 00h the periods are consistent.

8.2.2.3 TF: timer flag

The timer flag (bit TF) is set logic 1 on the first trigger of MI, HMI, or the countdown timer. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: timer or alarm. The flag can be read and cleared by command.

The status of the timer flag TF can affect the $\overline{\text{INT}}$ pulse generation depending on the setting of TI_TP (see [Section 8.6.2 “Register Timer_mode” on page 27](#)):

- When TI_TP is set logic 1
 - an $\overline{\text{INT}}$ pulse is generated independent of the status of the timer flag TF
 - TF stays set until it is cleared
 - TF does not affect $\overline{\text{INT}}$
 - the countdown timer runs in a repetitive loop and keeps generating timed periods
- When TI_TP is set logic 0
 - the $\overline{\text{INT}}$ generation follows the TF flag
 - TF stays set until it is cleared
 - If TF is not cleared before the next coming interrupt, no $\overline{\text{INT}}$ is generated
 - the countdown timer stops after the first countdown

8.2.2.4 COF[2:0]: Clock output frequency

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Control_2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting COF[2:0] to 111 or by setting CLKOE LOW. When disabled, the CLKOUT is LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all are 50 : 50 except the 32.768 kHz frequencies.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function, see [Section 8.2.1.2](#).

Table 11. CLKOUT frequency selection

| COF[2:0] | CLKOUT frequency (Hz) | Typical duty cycle ^[1] | Effect of STOP bit |
|--------------------|-----------------------|-----------------------------------|--------------------|
| 000 ^[2] | 32768 | 60 : 40 to 40 : 60 | no effect |
| 001 | 16384 | 50 : 50 | no effect |
| 010 | 8192 | 50 : 50 | no effect |
| 011 | 4096 | 50 : 50 | CLKOUT = LOW |
| 100 | 2048 | 50 : 50 | CLKOUT = LOW |
| 101 | 1024 | 50 : 50 | CLKOUT = LOW |
| 110 | 1 ^[3] | 50 : 50 | CLKOUT = LOW |
| 111 | CLKOUT = LOW | - | - |

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] 1 Hz clock pulses are affected by offset correction pulses.

8.2.3 Register Offset

The PCF85063BTL incorporates an offset register (address 02h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Table 12. Offset - offset register (address 02h) bit description

| Bit | Symbol | Value | Description |
|--------|-------------|------------------------------|--|
| 7 | MODE | | offset mode |
| | | 0 ^[1] | normal mode: offset is made once every two hours |
| | | 1 | course mode: offset is made every 4 minutes |
| 6 to 0 | OFFSET[6:0] | see Table 13 | offset value |

[1] Default value.

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The values of 4.34 ppm and 4.069 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

Table 13. Offset values

| OFFSET[6:0] | Offset value in decimal | Offset value in ppm | |
|------------------------|-------------------------|-------------------------|-----------------------|
| | | Normal mode MODE = 0 | Fast mode MODE = 1 |
| 0111111 | +63 | +273.420 | +256.347 |
| 0111110 | +62 | +269.080 | +252.278 |
| : | : | : | : |
| 0000010 | +2 | +8.680 | +8.138 |
| 0000001 | +1 | +4.340 | +4.069 |
| 0000000 ^[1] | 0 | 0 ^[1] | 0 ^[1] |
| 1111111 | -1 | -4.340 | -4.069 |
| 1111110 | -2 | -8.680 | -8.138 |
| : | : | : | : |
| 1000001 | -63 | -273.420 | -256.347 |
| 1000000 | -64 | -277.760 | -260.416 |

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control_1) has to be set logic 1. At every correction cycle a pulse is generated on pin $\overline{\text{INT}}$. The pulse width depends on the correction mode. If multiple correction pulses are applied, an interrupt pulse is generated for each correction pulse applied.

8.2.3.1 Correction when MODE = 0

The correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 14. Correction pulses for MODE = 0

| Correction value | Update every n th hour | Minute | Correction pulses on INT per minute ^[1] |
|------------------|-----------------------------------|--------------------|--|
| +1 or -1 | 2 | 00 | 1 |
| +2 or -2 | 2 | 00 and 01 | 1 |
| +3 or -3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or -59 | 2 | 00 to 58 | 1 |
| +60 or -60 | 2 | 00 to 59 | 1 |
| +61 or -61 | 2 | 00 to 59 | 1 |
| | 2nd and next hour | 00 | 1 |
| +62 or -62 | 2 | 00 to 59 | 1 |
| | 2nd and next hour | 00 and 01 | 1 |
| +63 or -63 | 02 | 00 to 59 | 1 |
| | 2nd and next hour | 00, 01, and 02 | 1 |
| -64 | 02 | 00 to 59 | 1 |
| | 2nd and next hour | 00, 01, 02, and 03 | 1 |

[1] The correction pulses on pin $\overline{\text{INT}}$ are $\frac{1}{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction (see [Table 15](#)).

Table 15. Effect of correction pulses on frequencies for MODE = 0

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | no effect |
| 1 | affected |
| $\frac{1}{60}$ | affected |

8.2.3.2 Correction when MODE = 1

The correction is triggered once every four minutes and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 16. Correction pulses for MODE = 1

| Correction value | Update every n th minute | Second | Correction pulses on INT per second ^[1] |
|------------------|-------------------------------------|----------------|--|
| +1 or -1 | 2 | 00 | 1 |
| +2 or -2 | 2 | 00 and 01 | 1 |
| +3 or -3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or -59 | 2 | 00 to 58 | 1 |
| +60 or -60 | 2 | 00 to 59 | 1 |
| +61 or -61 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 2 |
| +62 or -62 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 3 |
| +63 or -63 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 4 |
| -64 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 5 |

[1] The correction pulses on pin $\overline{\text{INT}}$ are $\frac{1}{1024}$ s wide. For multiple pulses, they are repeated at an interval of $\frac{1}{512}$ s.

In MODE = 1, any timer source clock using a frequency below 1.024 kHz is also affected by the clock correction (see [Table 17](#)).

Table 17. Effect of correction pulses on frequencies for MODE = 1

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | affected |
| 1 | affected |
| $\frac{1}{60}$ | affected |

8.2.3.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. [Figure 9](#) shows the workflow how the offset register values can be calculated:

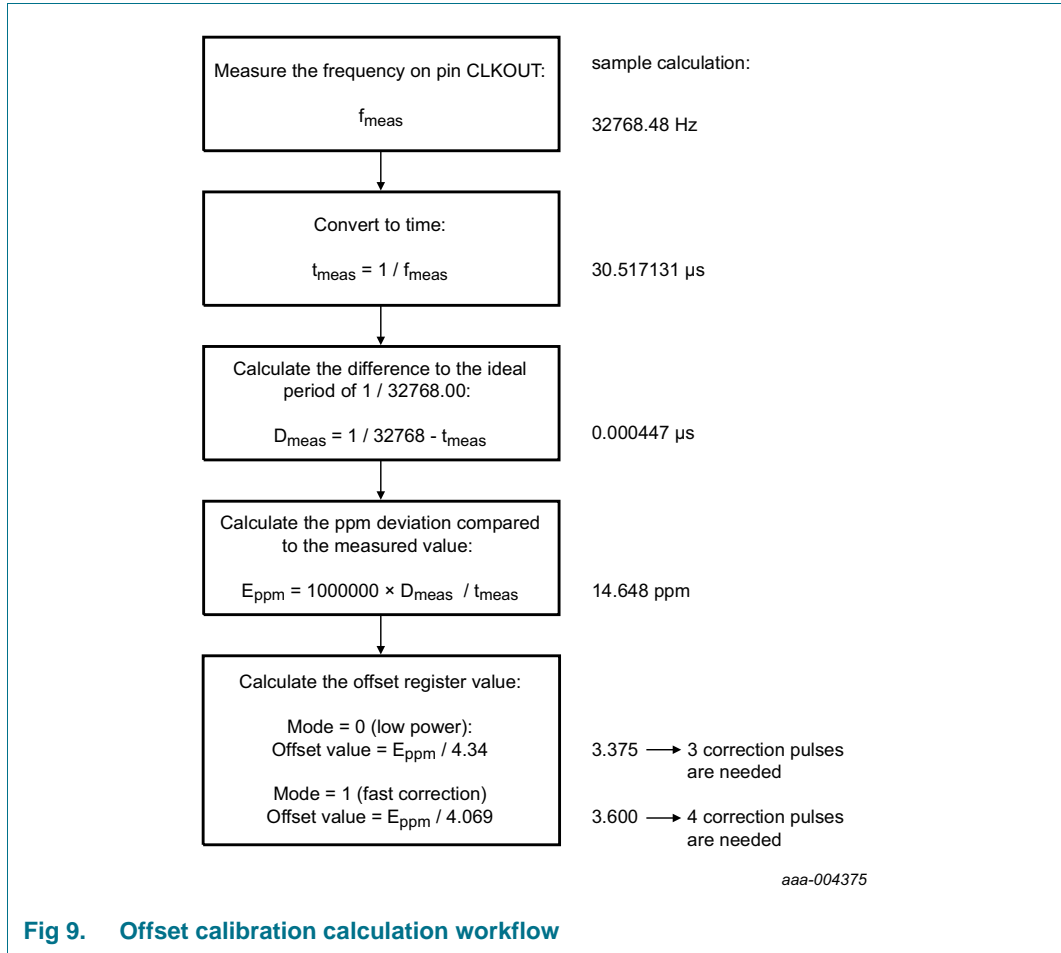
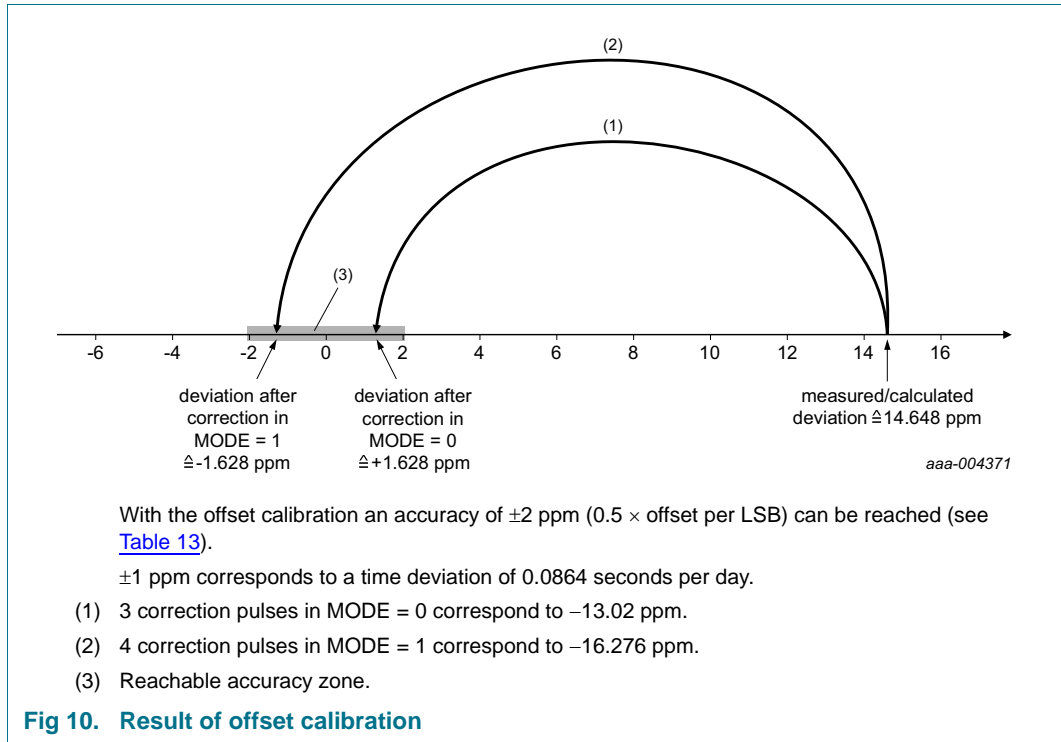


Fig 9. Offset calibration calculation workflow



8.2.4 Register RAM_byte

The PCF85063BTL provides a free RAM byte, which can be used for any purpose, for example, status byte of the system.

Table 18. RAM_byte - 8-bit RAM register (address 03h) bit description

| Bit | Symbol | Value | Description |
|--------|--------|-------------------------------------|-------------|
| 7 to 0 | B[7:0] | 00000000 ^[1] to 11111111 | RAM content |

[1] Default value.

8.3 Time and date registers

Most of the registers are coded in the BCD format to simplify application use.

8.3.1 Register Seconds

Table 19. Seconds - seconds register (address 04h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | OS | | | oscillator stop |
| | | 0 | - | clock integrity is guaranteed |
| | | 1 ^[1] | - | clock integrity is not guaranteed; oscillator has stopped or has been interrupted |
| 6 to 4 | SECONDS | 0 ^[1] to 5 | ten's place | actual seconds coded in BCD format, see Table 20 |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

Table 20. Seconds coded in BCD format

| Seconds value in decimal | Upper-digit (ten's place) | | | Digit (unit place) | | | |
|--------------------------|---------------------------|-------|-------|--------------------|-------|-------|-------|
| | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 ^[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : | : | : |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

[1] Default value.

8.3.1.1 OS flag: Oscillator stop

When the oscillator of the PCF85063BTL is stopped, the OS flag is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The flag remains set until cleared by command (see Figure 11). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

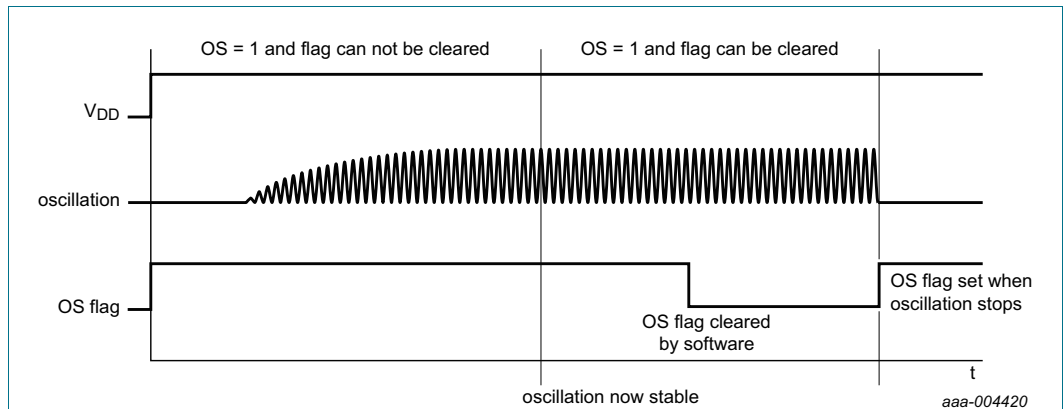


Fig 11. OS flag

8.3.2 Register Minutes

Table 21. Minutes - minutes register (address 05h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | - | 0 | - | unused |
| 6 to 4 | MINUTES | 0 ^[1] to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.3.3 Register Hours

Table 22. Hours - hours register (address 06h) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------------|--------|-----------------------|-------------|---|
| 7 to 6 | - | 00 | - | unused |
| 12 hour mode^[1] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[2] | - | AM |
| | | 1 | - | PM |
| 4 | HOURS | 0 ^[2] to 1 | ten's place | actual hours in 12 hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |
| 24 hour mode^[1] | | | | |
| 5 to 4 | HOURS | 0 ^[2] to 2 | ten's place | actual hours in 24 hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |

[1] Hour mode is set by the 12_24 bit in register Control_1.

[2] Default value.

8.3.4 Register Days

Table 23. Days - days register (address 07h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------------------|-----------------------|-------------|---------------------------------------|
| 7 to 6 | - | 00 | - | unused |
| 5 to 4 | DAYS ^[1] | 0 ^[2] to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 ^[3] to 9 | unit place | |

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the PCF85063BTL compensates for leap years by adding a 29th day to February.

[2] Default value.

[3] Default value is 1.

8.3.5 Register Weekdays

Table 24. Weekdays - weekdays register (address 08h) bit description

| Bit | Symbol | Value | Description |
|--------|----------|--------|--|
| 7 to 3 | - | 00000 | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 25 |

Table 25. Weekday assignments

| Day ^[1] | Bit | | |
|-------------------------|-----|---|---|
| | 2 | 1 | 0 |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday ^[2] | 1 | 1 | 0 |

[1] Definition may be reassigned by the user.

[2] Default value.

8.3.6 Register Months

Table 26. Months - months register (address 09h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|--------|-------------|---|
| 7 to 5 | - | 000 | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 27 |
| 3 to 0 | | 0 to 9 | unit place | |

Table 27. Month assignments in BCD format

| Month | Upper-digit (ten's place) | Digit (unit place) | | | |
|------------------------|------------------------------|--------------------|-------|-------|-------|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January ^[1] | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

[1] Default value.

8.3.7 Register Years

Table 28. Years - years register (0Ah) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|-----------------------|-------------|--|
| 7 to 4 | YEARS | 0 ^[1] to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.4 Setting and reading the time

Figure 12 shows the data flow and data dependencies starting from the 1 Hz clock tick.

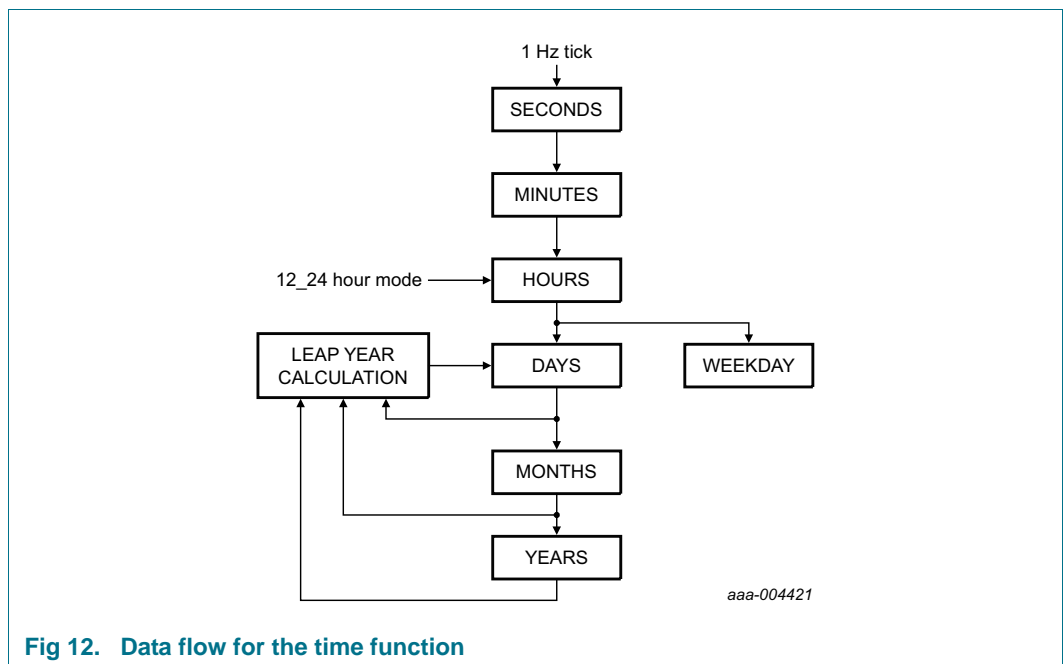


Fig 12. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 04h through 0Ah) are blocked.

The blocking prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 13).

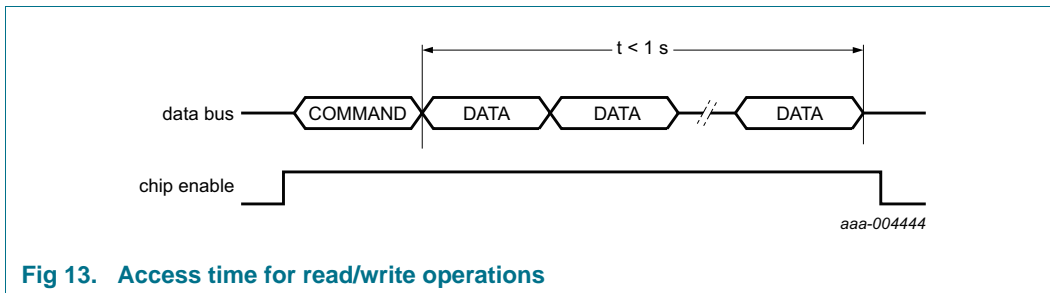


Fig 13. Access time for read/write operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send read command with register address pointing to 4 (Seconds) by sending 04h
2. Read Seconds
3. Read Minutes
4. Read Hours
5. Read Days
6. Read Weekdays
7. Read Months
8. Read Years

8.5 Alarm registers

8.5.1 Register Second_alarm

Table 29. Second_alarm - second alarm register (address 0Bh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|--|
| 7 | AEN_S | | | second alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | SECOND_ALARM | 0 ^[1] to 5 | ten's place | second alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.2 Register Minute_alarm

Table 30. Minute_alarm - minute alarm register (address 0Ch) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|--|
| 7 | AEN_M | | | minute alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | MINUTE_ALARM | 0 ^[1] to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.3 Register Hour_alarm

Table 31. Hour_alarm - hour alarm register (address 0Dh) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------------|------------|-----------------------|-------------|--|
| 7 | AEN_H | | | hour alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 12 hour mode^[2] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[1] | - | AM |
| | | 1 | - | PM |
| 4 | HOUR_ALARM | 0 ^[1] to 1 | ten's place | hour alarm information in 12 hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |
| 24 hour mode^[2] | | | | |
| 5 to 4 | HOUR_ALARM | 0 ^[1] to 2 | ten's place | hour alarm information in 24 hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

[2] Hour mode is set by the 12_24 bit in register Control_1.

8.5.4 Register Day_alarm

Table 32. Day_alarm - day alarm register (address 0Eh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|-----------|-----------------------|-------------|--|
| 7 | AEN_D | | | day alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 5 to 4 | DAY_ALARM | 0 ^[1] to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.5 Register Weekday_alarm

Table 33. Weekday_alarm - weekday alarm register (address 0Fh) bit description

| Bit | Symbol | Value | Description |
|--------|---------------|-----------------------|--|
| 7 | AEN_W | | weekday alarm |
| | | 0 | enabled |
| | | 1 ^[1] | disabled |
| 6 to 3 | - | 0 | unused |
| 2 to 0 | WEEKDAY_ALARM | 0 ^[1] to 6 | weekday alarm information coded in BCD format |

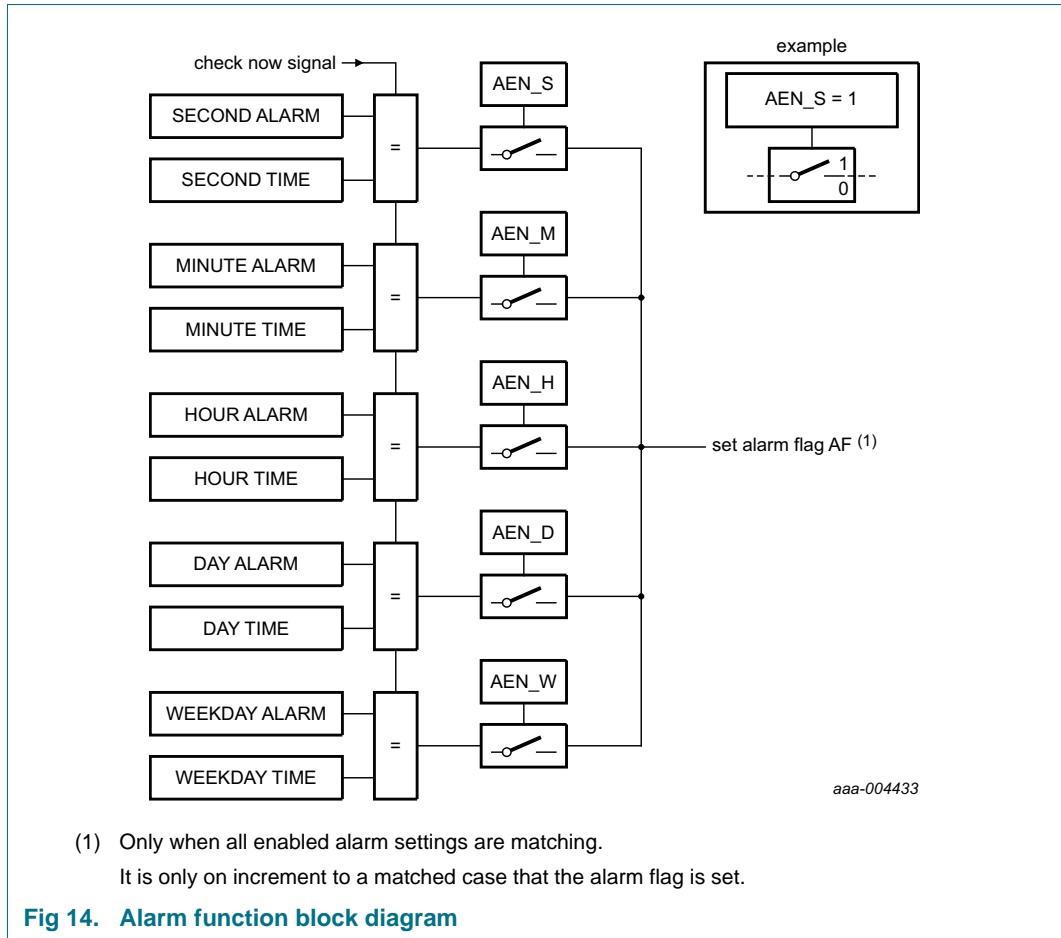
[1] Default value.

8.5.6 Alarm function

By clearing the alarm enable bit (AEN_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set logic 1. The asserted AF can be used to generate an interrupt (INT). The AF is cleared by command.

The registers at addresses 0Bh through 0Fh contain alarm information. When one or more of these registers is loaded with second, minute, hour, day or weekday, and its corresponding AEN_x is logic 0, then that information is compared with the current second, minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the INT pin follows the condition of bit AF. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_x bit at logic 1 are ignored.



8.6 Timer registers

The 8-bit countdown timer at address 10h is controlled by the register `Timer_mode` at address 11h.

8.6.1 Register `Timer_value`

Table 34. `Timer_value` - timer value register (address 10h) bit description

| Bit | Symbol | Value | Description |
|--------|--------|--------------------------|--------------------------------------|
| 7 to 0 | T[7:0] | 0h ^[1] to FFh | countdown timer value ^[2] |

[1] Default value.

[2] Countdown period in seconds: $CountdownPeriod = \frac{T}{SourceClockFrequency}$ where T is the countdown value.

8.6.2 Register `Timer_mode`

Table 35. `Timer_mode` - timer control register (address 11h) bit description

| Bit | Symbol | Value | Description |
|--------|----------------------|-------------------|--------------------------------------|
| 7 to 5 | - | 000 | unused |
| 4 to 3 | TCF[1:0] | | timer clock frequency |
| | | 00 | 4.096 kHz timer source clock |
| | | 01 | 64 Hz timer source clock |
| | | 10 | 1 Hz timer source clock |
| | | 11 ^[1] | $\frac{1}{60}$ Hz timer source clock |
| 2 | TE | | timer enable |
| | | 0 ^[1] | timer is disabled |
| | | 1 | timer is enabled |
| 1 | TIE | | timer interrupt enable |
| | | 0 ^[1] | no interrupt generated from timer |
| | | 1 | interrupt generated from timer |
| 0 | TI_TP ^[2] | | timer interrupt mode |
| | | 0 ^[1] | interrupt follows timer flag |
| | | 1 | interrupt generates a pulse |

[1] Default value.

[2] How the setting of `TI_TP` and the timer flag `TF` can affect the \overline{INT} pulse generation is explained in [Section 8.2.2.3 on page 12](#).

8.6.3 Timer functions

The timer has four selectable source clocks allowing for countdown periods in the range from 244 μ s to 4 hours 15 min. For periods longer than 4 hours, the alarm function can be used.

Table 36. Timer clock frequency and timer durations

| TCF[1:0] | Timer source clock frequency ^[1] | Delay | |
|----------|---|---------------------------------|-----------------------------------|
| | | Minimum timer duration T = 1 | Maximum timer duration T = 255 |
| 00 | 4.096 kHz | 244 μs | 62.256 ms |
| 01 | 64 Hz | 15.625 ms | 3.984 s |
| 10 | 1 Hz ^[2] | 1 s | 255 s |
| 11 | 1/60 Hz ^[2] | 60 s | 4 hours 15 min |

[1] When not in use, TCF[1:0] must be set to 1/60 Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, T[7:0], in register Timer_value. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid.

When the counter decrements from 1, the timer flag (bit TF in register Control_2) is set and the counter automatically re-loads and starts the next timer period.

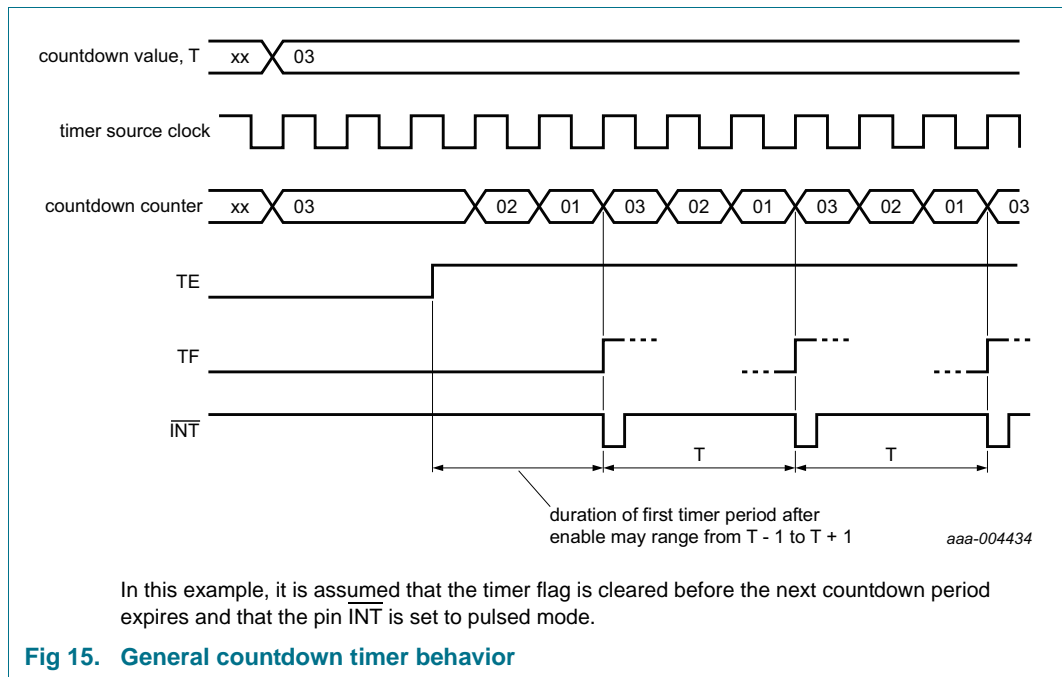


Fig 15. General countdown timer behavior

If a new value of T is written before the end of the current timer period, then this value takes immediate effect. NXP does not recommend changing T without first disabling the counter by setting bit TE logic 0. The update of T is asynchronous to the timer clock. Therefore changing it without setting bit TE logic 0 may result in a corrupted value loaded into the countdown counter. This results in an undetermined countdown period for the first period. The countdown value T will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the TIE flag is set, an interrupt signal on $\overline{\text{INT}}$ is generated if this mode is enabled. See [Section 8.2.2](#) for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods do not have such delay. The amount of delay for the first timer period depends on the chosen source clock, see [Table 37](#).

Table 37. First period delay for timer counter value T

| Timer source clock | Minimum timer period | Maximum timer period |
|--------------------|-------------------------------------|-------------------------------|
| 4.096 kHz | T | T + 1 |
| 64 Hz | T | T + 1 |
| 1 Hz | $(T - 1) + \frac{1}{64 \text{ Hz}}$ | $T + \frac{1}{64 \text{ Hz}}$ |
| $\frac{1}{60}$ Hz | $(T - 1) + \frac{1}{64 \text{ Hz}}$ | $T + \frac{1}{64 \text{ Hz}}$ |

At the end of every countdown, the timer sets the countdown timer flag (bit TF in register Control_2). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt at pin $\overline{\text{INT}}$. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see [Table 35](#) and [Figure 15](#).

When reading the timer, the current countdown value is returned and **not** the initial value T. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and $\frac{1}{60}$ Hz is affected by the Offset register. The duration of a program period varies according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefore be longer or shorter depending on the setting of the Offset register. See [Section 8.2.3](#) to understand the operation of the Offset register.

8.6.3.1 Countdown timer interrupts

The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies (see [Table 38](#)).

Table 38. $\overline{\text{INT}}$ operation
TF and $\overline{\text{INT}}$ become active simultaneously.

| Source clock (Hz) | $\overline{\text{INT}}$ period (s) | |
|-------------------|------------------------------------|----------------------|
| | T = 1 ^[1] | T > 1 ^[1] |
| 4096 | $\frac{1}{8192}$ | $\frac{1}{4096}$ |
| 64 | $\frac{1}{128}$ | $\frac{1}{64}$ |
| 1 | $\frac{1}{64}$ | $\frac{1}{64}$ |
| $\frac{1}{60}$ | $\frac{1}{64}$ | $\frac{1}{64}$ |

[1] T = loaded countdown value. Timer stops when T = 0.

9. Characteristics of the SPI-bus interface

Data transfer to and from the device is made via a 3-wire SPI-bus (see [Table 39](#)). The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first (see [Figure 16](#)).

Table 39. Serial interface

| Symbol | Function | Description |
|--------|------------------------------|---|
| CE | chip enable input | when LOW, the interface is reset; pull-down resistor included; active input may be higher than V_{DD} , but may not be wired permanently HIGH |
| SCL | serial clock input | when CE is LOW, this input may float; input may be higher than V_{DD} |
| SDIO | serial data input and output | |
| | input | when CE is LOW, input may float; input may be higher than V_{DD} ; input data is sampled on the rising edge of SCL |
| | output | push-pull output; drives from V_{SS} to V_{DD} ; output data is changed on the falling edge of SCL; is high-impedance when not driving |

The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes are either data to be written or data to be read. Data is sampled on the rising edge of the clock and transferred internally on the falling edge.

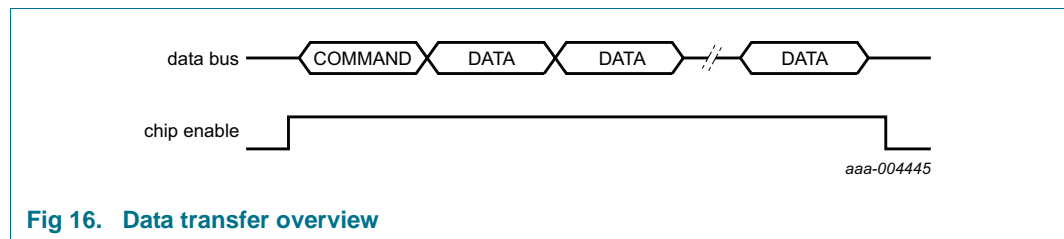


Fig 16. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will roll over to zero after the last register is accessed (see [Figure 3](#)). The (R/W) bit defines whether the following bytes are read or write information.

Table 40. Command byte definition

| Bit | Symbol | Value | Description |
|--------|------------------|-----------|---|
| 7 | R/\overline{W} | | data read or data write selection |
| | | 0 | write data |
| | | 1 | read data |
| 6 to 5 | SA | 01 | subaddress ; other codes will cause the device to ignore data transfer |
| 4 to 0 | RA | 0h to 11h | register address range ; other addresses will be ignored |

In [Figure 17](#), the register Seconds is set to 45 seconds and the register Minutes is set to 10 minutes. In [Figure 18](#), the Months and Years registers are read.

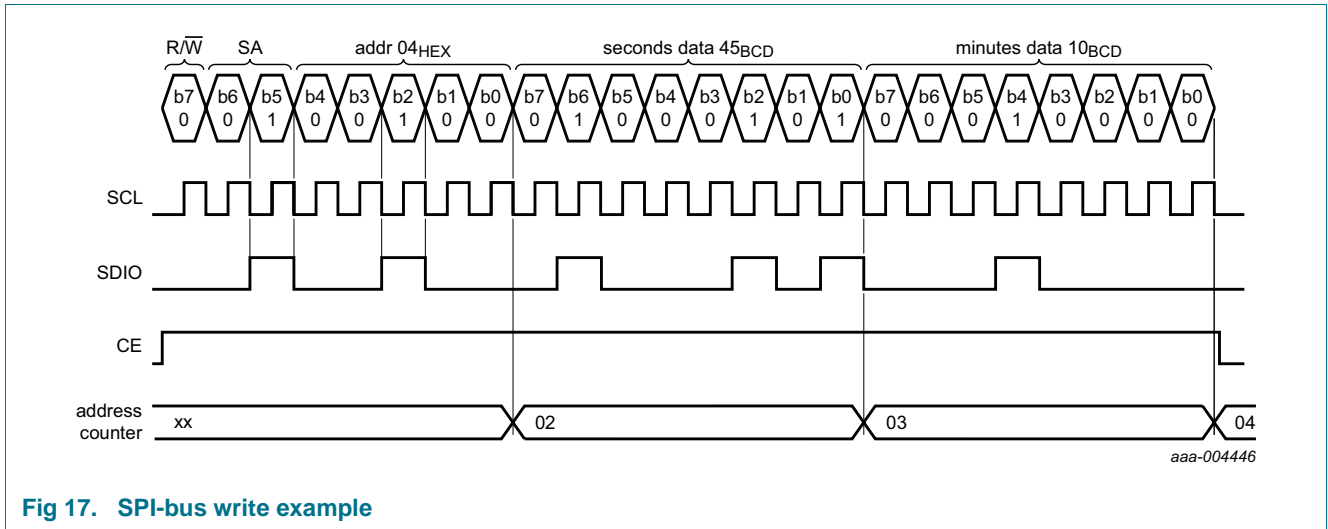


Fig 17. SPI-bus write example

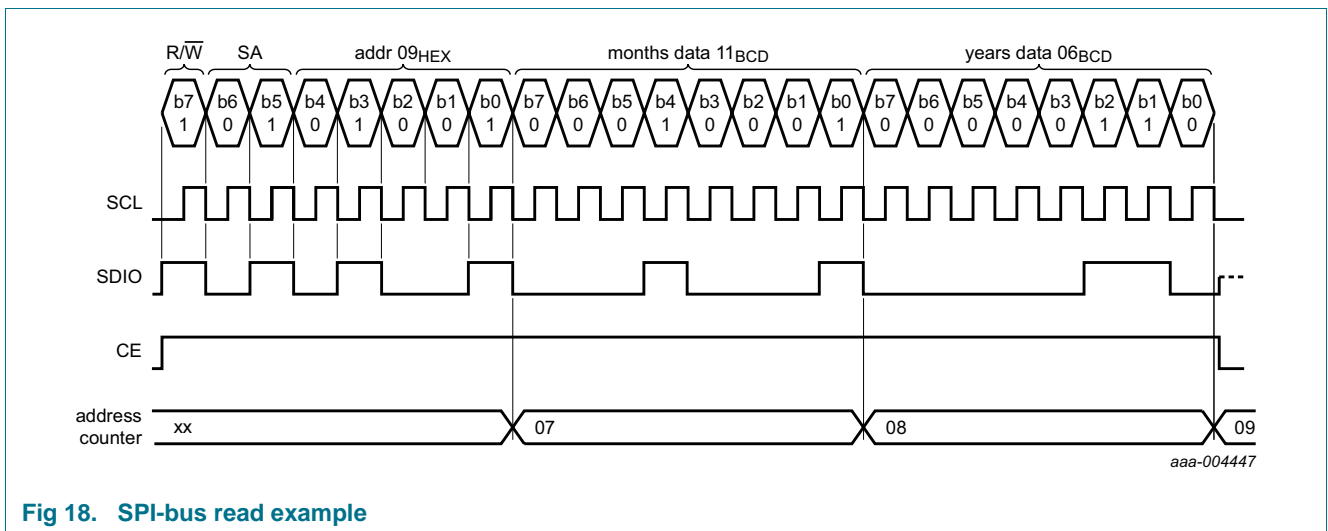


Fig 18. SPI-bus read example

10. Internal circuitry

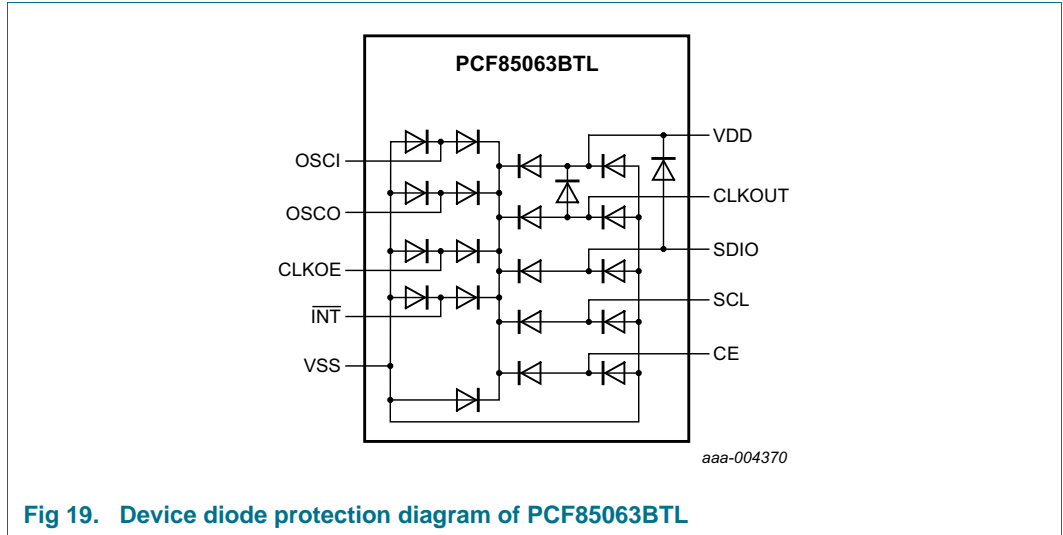


Fig 19. Device diode protection diagram of PCF85063BTL

11. Limiting values

Table 41. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------|---------------------------------|-------------------------|------|------|-------|----|
| V_{DD} | supply voltage | | -0.5 | +6.5 | V | |
| I_{DD} | supply current | | -50 | +50 | mA | |
| V_I | input voltage | on pins SCL, SDIO, OSCI | -0.5 | +6.5 | V | |
| V_O | output voltage | | -0.5 | +6.5 | V | |
| I_I | input current | at any input | -10 | +10 | mA | |
| I_O | output current | at any output | -10 | +10 | mA | |
| P_{tot} | total power dissipation | | - | 300 | mW | |
| V_{ESD} | electrostatic discharge voltage | HBM | [1] | - | ±5000 | V |
| | | CDM | [2] | - | ±2000 | V |
| I_{lu} | latch-up current | | [3] | - | 200 | mA |
| T_{stg} | storage temperature | | [4] | -65 | +150 | °C |
| T_{amb} | ambient temperature | operating device | -40 | +85 | °C | |

[1] Pass level; Human Body Model (HBM) according to [Ref. 7 "JESD22-A114"](#).

[2] Pass level; Charged-Device Model (CDM), according to [Ref. 8 "JESD22-C101"](#).

[3] Pass level; latch-up testing, according to [Ref. 9 "JESD78"](#) at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see [Ref. 12 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12. Characteristics

Table 42. Static characteristics

$V_{DD} = 0.9\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 60\text{ k}\Omega$; $C_L = 7\text{ pF}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------------|---|--|-------------|-----|---------------|---------------|----|
| Supplies | | | | | | | |
| V_{DD} | supply voltage | interface inactive; $f_{SCL} = 0\text{ MHz}$ | [1] 0.9 | - | 5.5 | V | |
| | | interface active; $f_{SCL} = 1\text{ MHz}$ | [1] 1.8 | - | 5.5 | V | |
| I_{DD} | supply current | CLKOUT disabled; $V_{DD} = 3.3\text{ V}$ | [2] | | | | |
| | | interface inactive; $f_{SCL} = 0\text{ Hz}$ | | | | | |
| | | $T_{amb} = 25\text{ °C}$ | - | 220 | 450 | nA | |
| | | $T_{amb} = 50\text{ °C}$ | [3] | - | 250 | 500 | nA |
| | | $T_{amb} = 85\text{ °C}$ | - | 470 | 600 | nA | |
| | interface active; $f_{SCL} = 1\text{ MHz}$ | - | 45 | 200 | μA | | |
| Inputs | | | | | | | |
| V_I | input voltage | | V_{SS} | - | 5.5 | V | |
| V_{IL} | LOW-level input voltage | | V_{SS} | - | $0.3V_{DD}$ | V | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | - | V_{DD} | V | |
| I_{LI} | input leakage current | $V_I = V_{SS}$ or V_{DD} | - | 0 | - | μA | |
| | | post ESD event | -0.15 | - | +0.15 | μA | |
| C_i | input capacitance | on pins SDIO, SCL, CE, CLKOE | [4] | - | 7 | pF | |
| Outputs | | | | | | | |
| V_{OH} | HIGH-level output voltage | on pins SDIO, CLKOUT | $0.8V_{DD}$ | - | V_{DD} | V | |
| V_{OL} | LOW-level output voltage | on pins SDIO, $\overline{\text{INT}}$, CLKOUT | V_{SS} | - | $0.2V_{DD}$ | V | |
| I_{OH} | HIGH-level output current | output source current; $V_{OH} = 2.9\text{ V}$; $V_{DD} = 3.3\text{ V}$ | | | | | |
| | | on pin SDIO | 2 | 5 | - | mA | |
| | | on pin CLKOUT | 1 | 3 | - | mA | |
| I_{OL} | LOW-level output current | output sink current; $V_{OL} = 0.4\text{ V}$; $V_{DD} = 3.3\text{ V}$ | | | | | |
| | | on pins SDIO, $\overline{\text{INT}}$ | 2 | 6 | - | mA | |
| | | on pin CLKOUT | 1 | 3 | - | mA | |

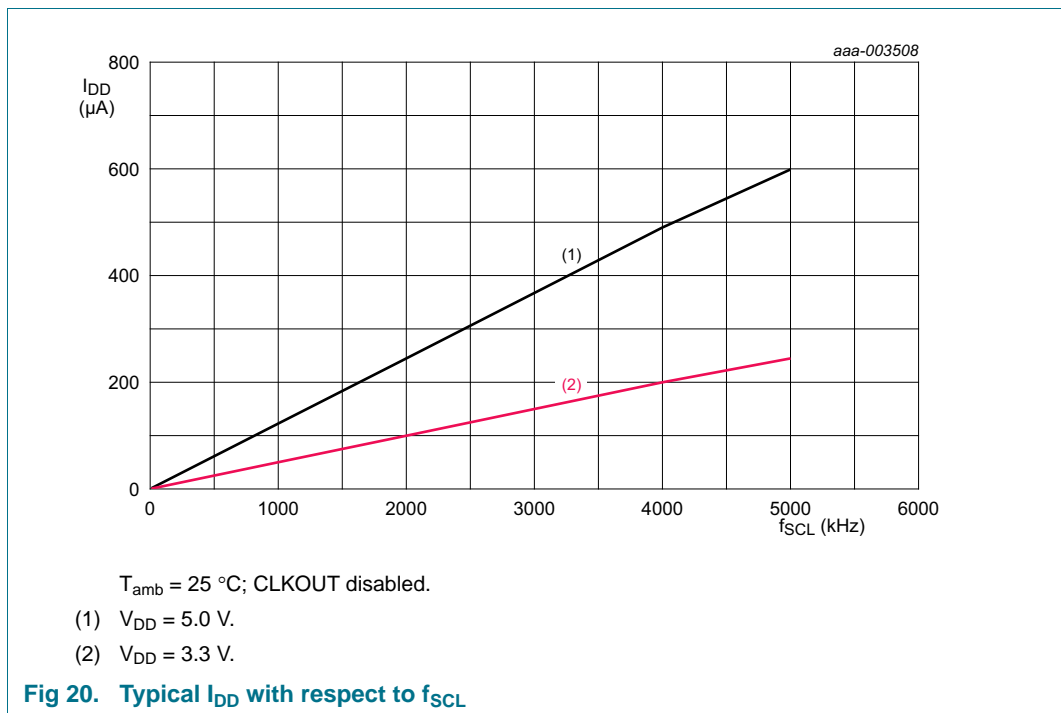
Table 42. Static characteristics ...continued

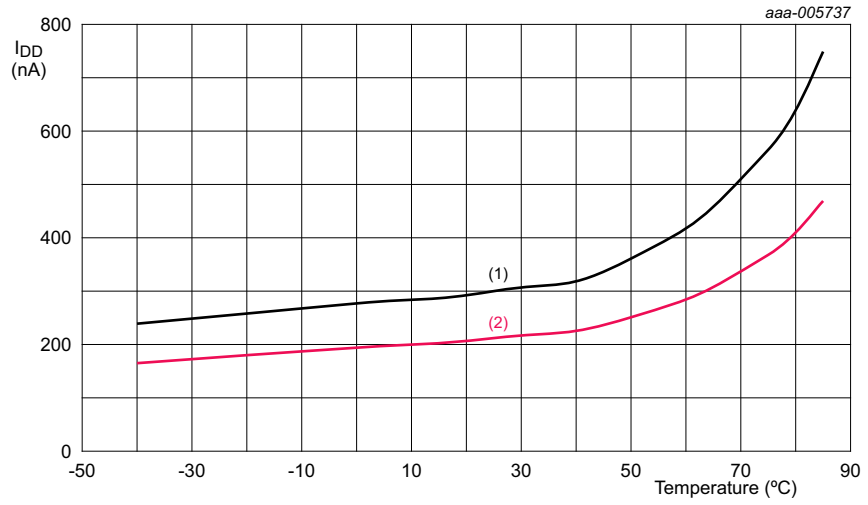
$V_{DD} = 0.9\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 60\text{ k}\Omega$; $C_L = 7\text{ pF}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|---|---|-----|-------|------|------------|
| Oscillator | | | | | | |
| $\Delta f_{osc}/f_{osc}$ | relative oscillator frequency variation | $\Delta V_{DD} = 200\text{ mV}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 0.075 | - | ppm |
| $C_{L(itg)}$ | integrated load capacitance | on pins OSCO, OSC1 | [5] | | | |
| | | $C_L = 7\text{ pF}$ | 4.2 | 7 | 9.8 | pF |
| | | $C_L = 12.5\text{ pF}$ | 7.5 | 12.5 | 17.5 | pF |
| R_s | series resistance | | - | - | 100 | k Ω |

- [1] For reliable oscillator start at power-on: $V_{DD} = V_{DD(po)sit}$ min + 0.3 V.
- [2] Timer source clock = $1/60$ Hz, level of pins CE, SDIO, and SCL is V_{DD} or V_{SS} .
- [3] Tested on sample basis.
- [4] Implicit by design.

[5] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

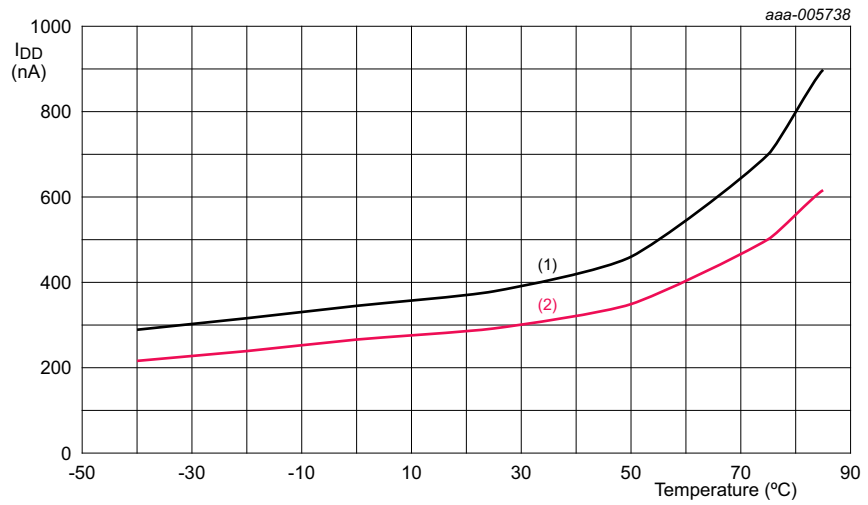




$C_{L(itg)} = 7$ pF; CLKOUT disabled.

(1) $V_{DD} = 5.5$ V.

(2) $V_{DD} = 3.3$ V.

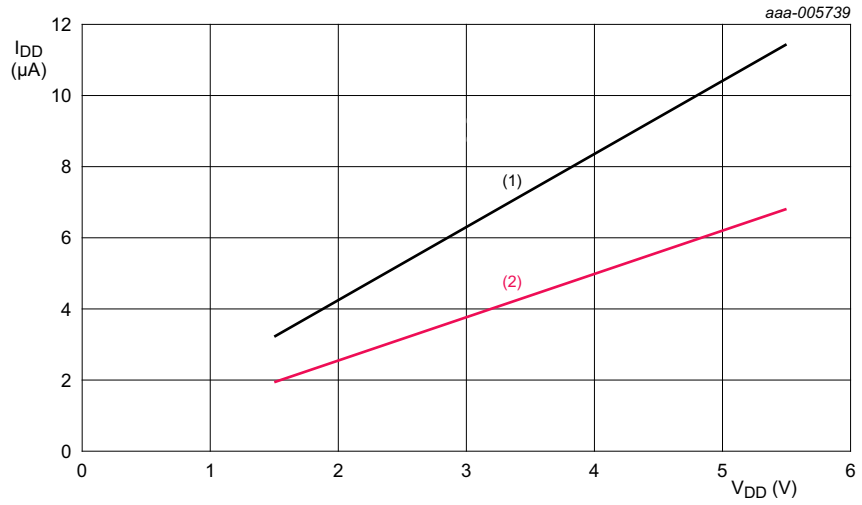


$C_{L(itg)} = 12.5$ pF; CLKOUT disabled.

(1) $V_{DD} = 5.5$ V.

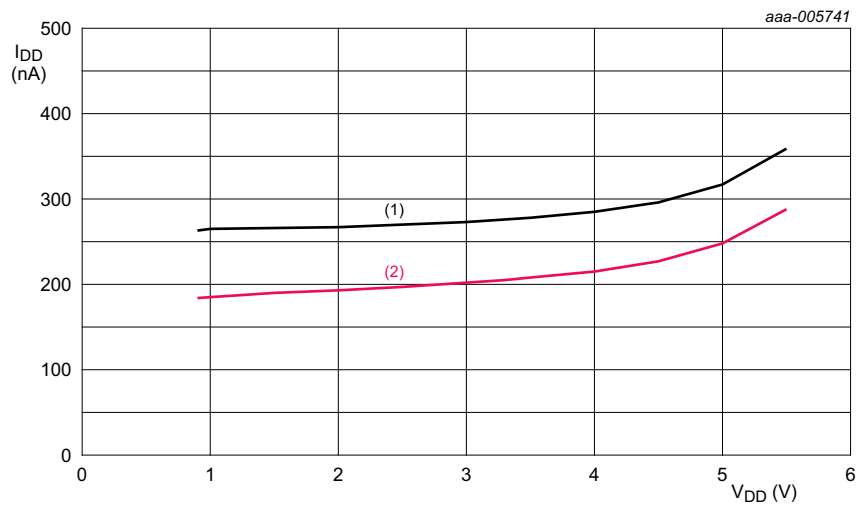
(2) $V_{DD} = 3.3$ V.

Fig 21. Typical I_{DD} as a function of temperature



$T_{amb} = 25\text{ }^{\circ}\text{C}$; $f_{CLKOUT} = 32768\text{ Hz}$.

- (1) 47 pF CLKOUT load.
- (2) 22 pF CLKOUT load.



$T_{amb} = 25\text{ }^{\circ}\text{C}$; CLKOUT disabled.

- (1) $C_{L(itg)} = 12.5\text{ pF}$.
- (2) $C_{L(itg)} = 7\text{ pF}$.

Fig 22. Typical I_{DD} with respect to V_{DD}

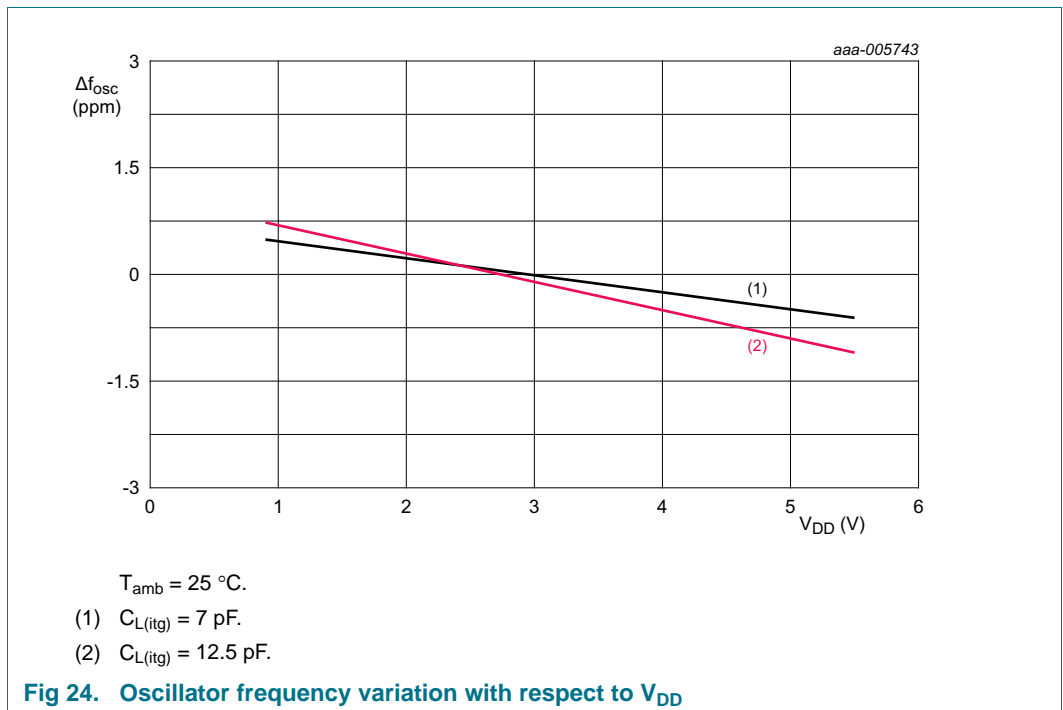
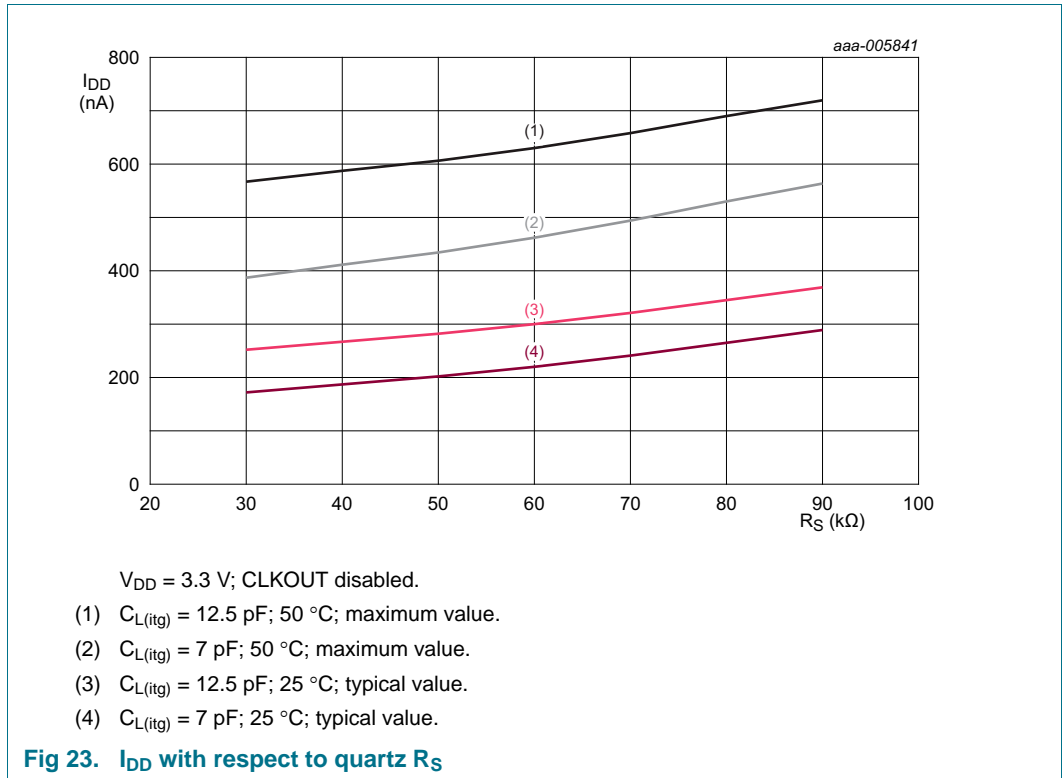


Table 43. SPI-bus characteristics

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 60\text{ k}\Omega$; $C_L = 7\text{ pF}$; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

| Symbol | Parameter | Conditions | $V_{DD} = 1.8\text{ V to }3.3\text{ V}$ | | $V_{DD} > 3.3\text{ V to }5.5\text{ V}$ | | Unit |
|------------------|---------------------------------|---|---|------|---|------|------|
| | | | Min | Max | Min | Max | |
| f_{SCL} | SCL clock frequency | | - | 5 | - | 7 | MHz |
| t_{SCL} | SCL time | | 140 | - | 140 | - | ns |
| $t_{clk(H)}$ | clock HIGH time | | 80 | - | 80 | - | ns |
| $t_{clk(L)}$ | clock LOW time | | 110 | - | 60 | - | ns |
| t_r | rise time | for SCL signal | - | 100 | - | 50 | ns |
| t_f | fall time | for SCL signal | - | 100 | - | 50 | ns |
| $t_{su(CE)}$ | CE set-up time | | 15 | - | 15 | - | ns |
| $t_{h(CE)}$ | CE hold time | | 10 | - | 10 | - | ns |
| $t_{rec(CE)}$ | CE recovery time | | 50 | - | 50 | - | ns |
| $t_w(CE)$ | CE pulse width | measured after valid subaddress is received | - | 0.99 | - | 0.99 | s |
| t_{su} | set-up time | set-up time for SDIO data | 5 | - | 5 | - | ns |
| t_h | hold time | hold time for SDIO data | 50 | - | 20 | - | ns |
| $t_{d(R)SDO}$ | SDO read delay time | bus load = 50 pF | - | 110 | - | 60 | ns |
| $t_{dis(SDO)}$ | SDO disable time | no load value; bus will be held up by bus capacitance; use RC time constant with application values | - | 50 | - | 50 | ns |
| $t_{t(SDI-SDO)}$ | transition time from SDI to SDO | to avoid bus conflict; on pin SDIO | 0 | - | 0 | - | ns |

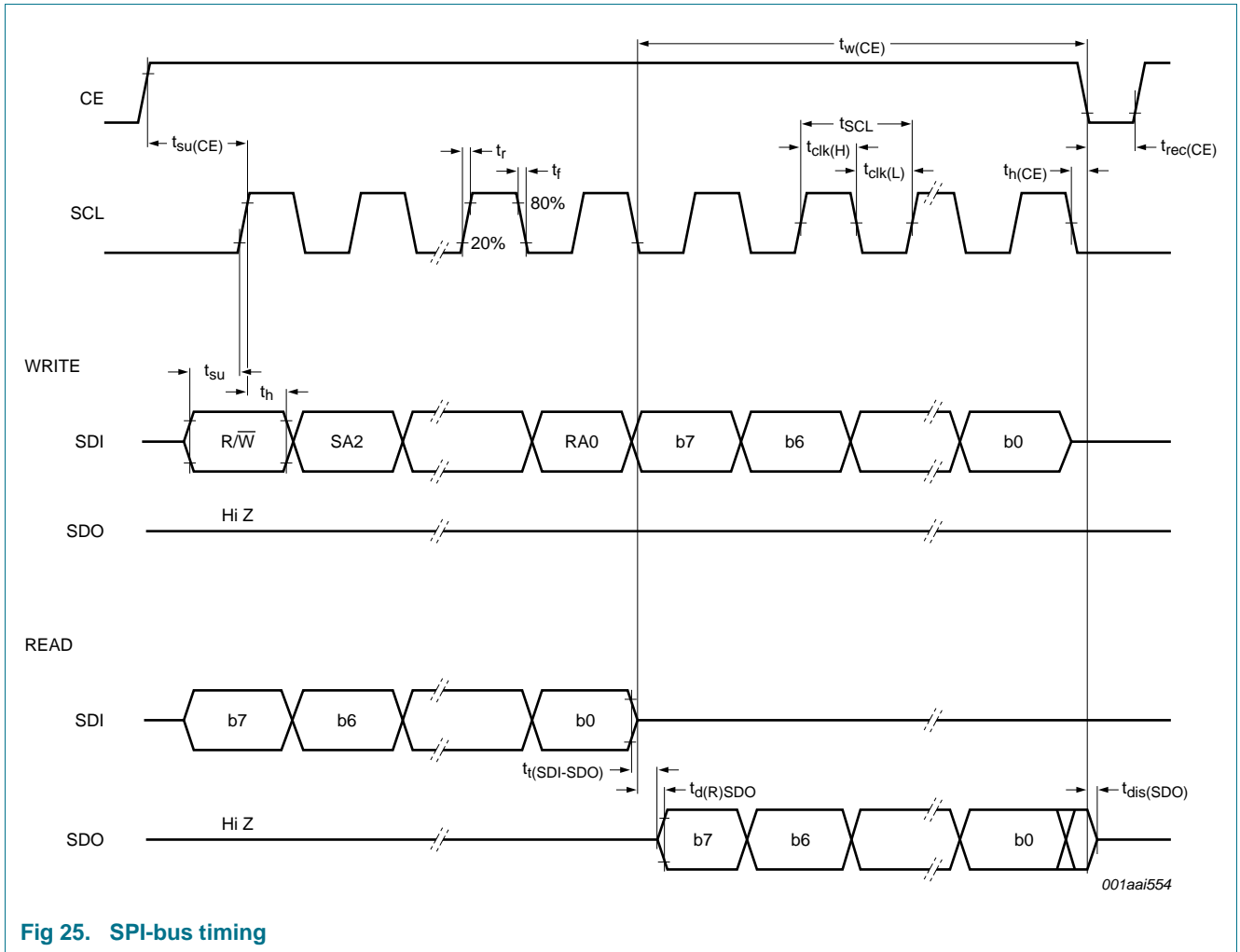
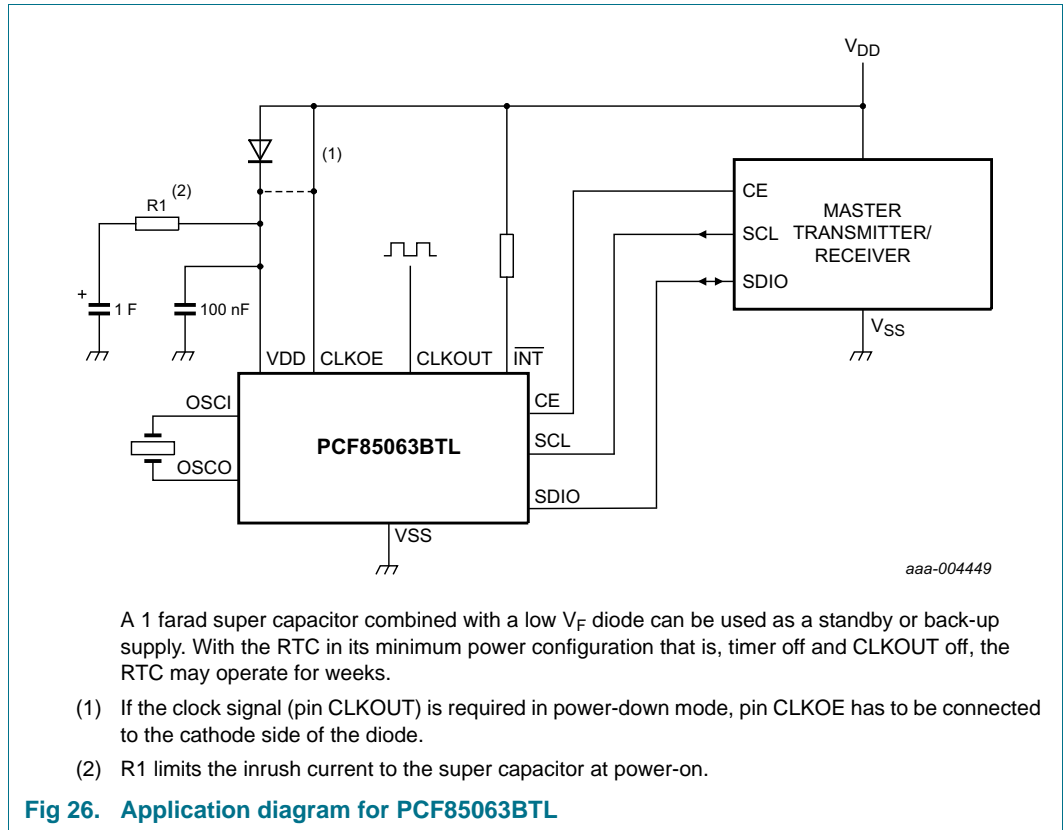


Fig 25. SPI-bus timing

13. Application information



14. Package outline

DFN2626-10: plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 x 2.6 x 0.5 mm

SOT1197-1

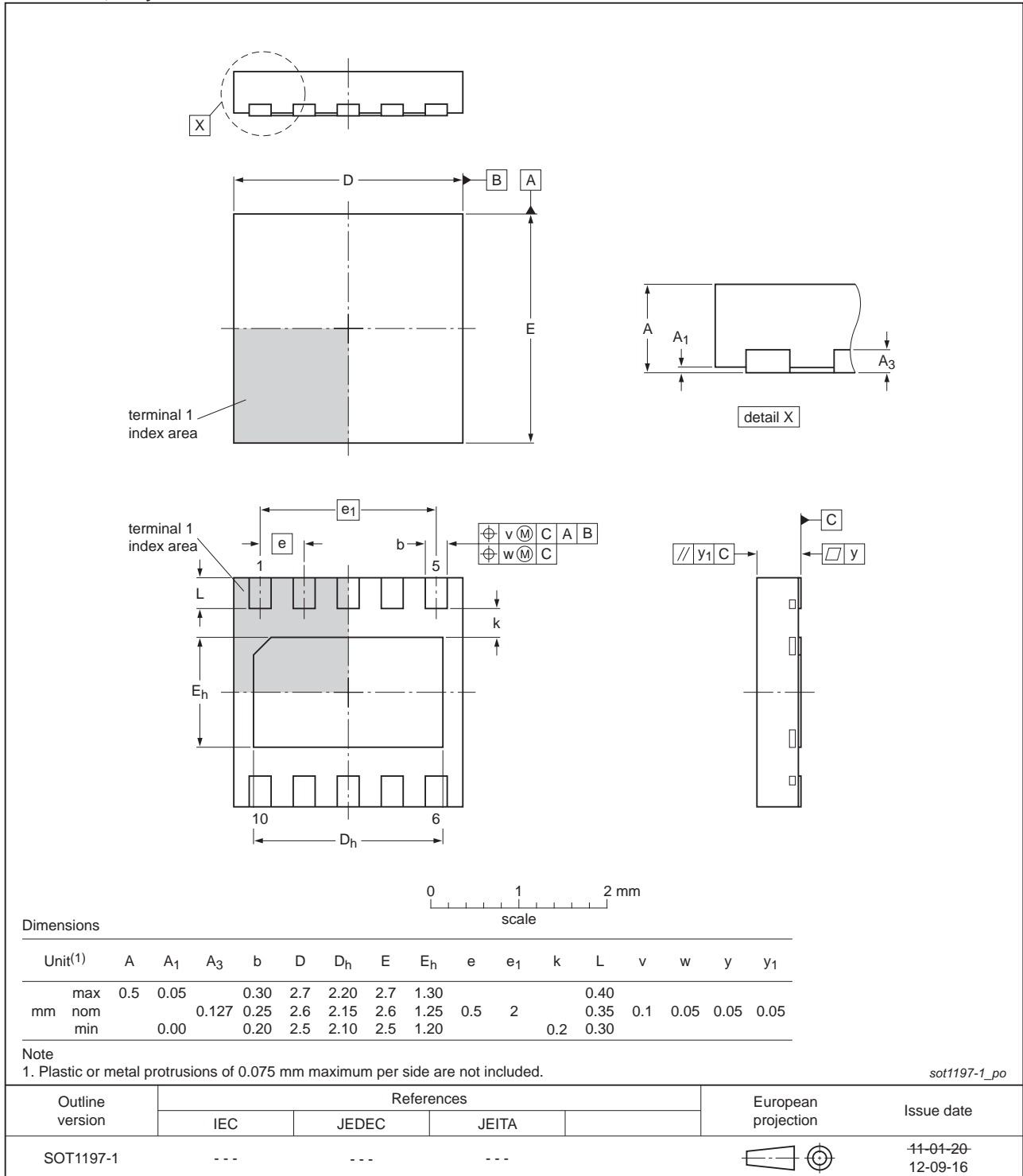


Fig 27. Package outline SOT1197-1 (HXSON10) of PCF85063BTL

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Tape and reel information

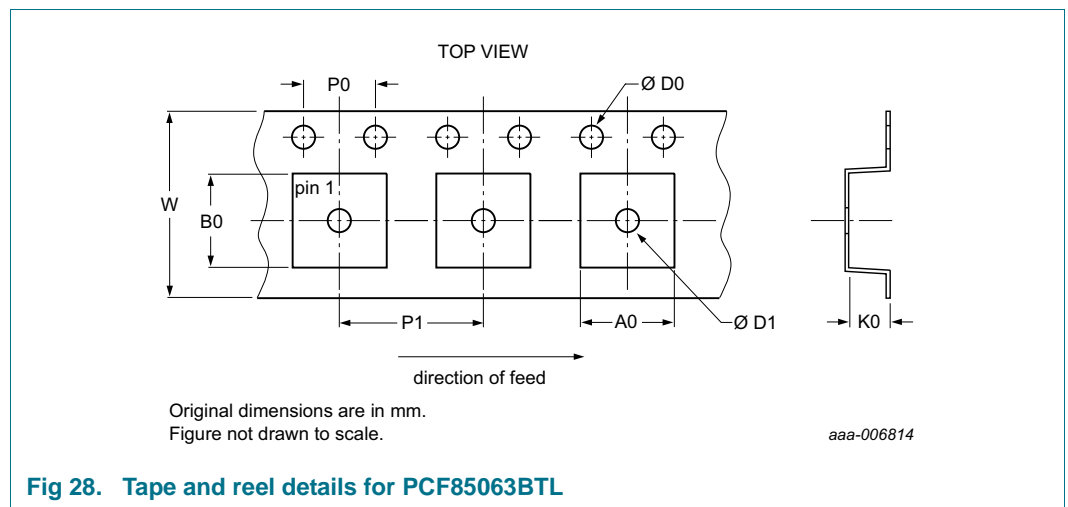


Fig 28. Tape and reel details for PCF85063BTL

Table 44. Carrier tape dimensions of PCF85063BTL

| Symbol | Description | Value | Unit |
|---------------------------|-----------------------------|-------|------|
| Compartments | | | |
| A0 | pocket width in x direction | 2.9 | mm |
| B0 | pocket width in y direction | 2.9 | mm |
| K0 | pocket depth | 0.8 | mm |
| P1 | pocket hole pitch | 4 | mm |
| D1 | pocket hole diameter | 1 | mm |
| Overall dimensions | | | |
| W | tape width | 8 | mm |
| D0 | sprocket hole diameter | 1.5 | mm |
| P0 | sprocket hole pitch | 4 | mm |

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 29](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 45](#) and [46](#)

Table 45. SnPb eutectic process (from J-STD-020D)

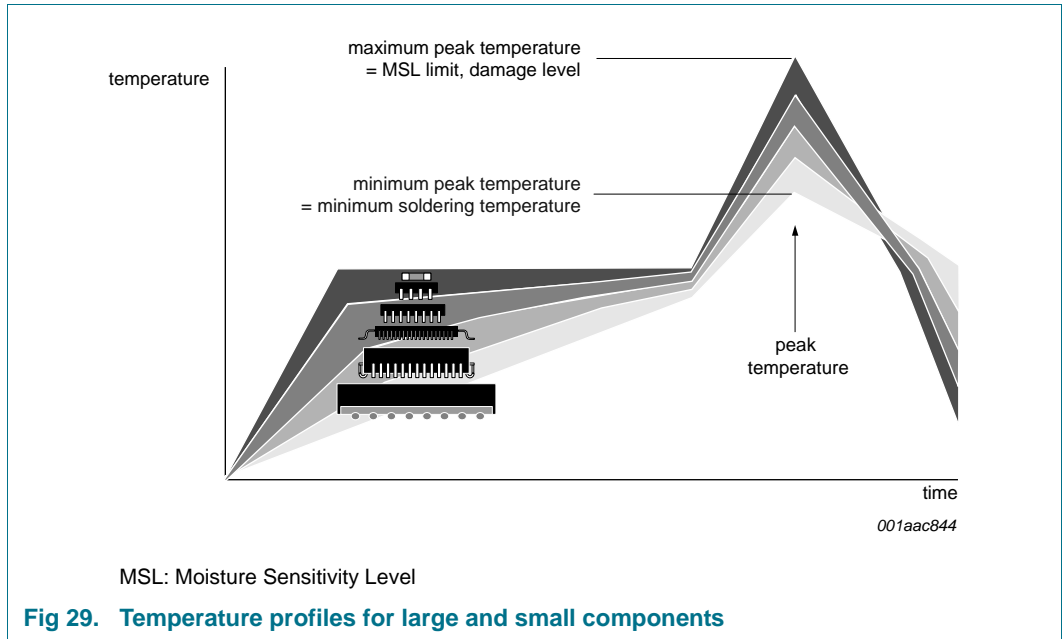
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 46. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 29](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

18. Footprint information

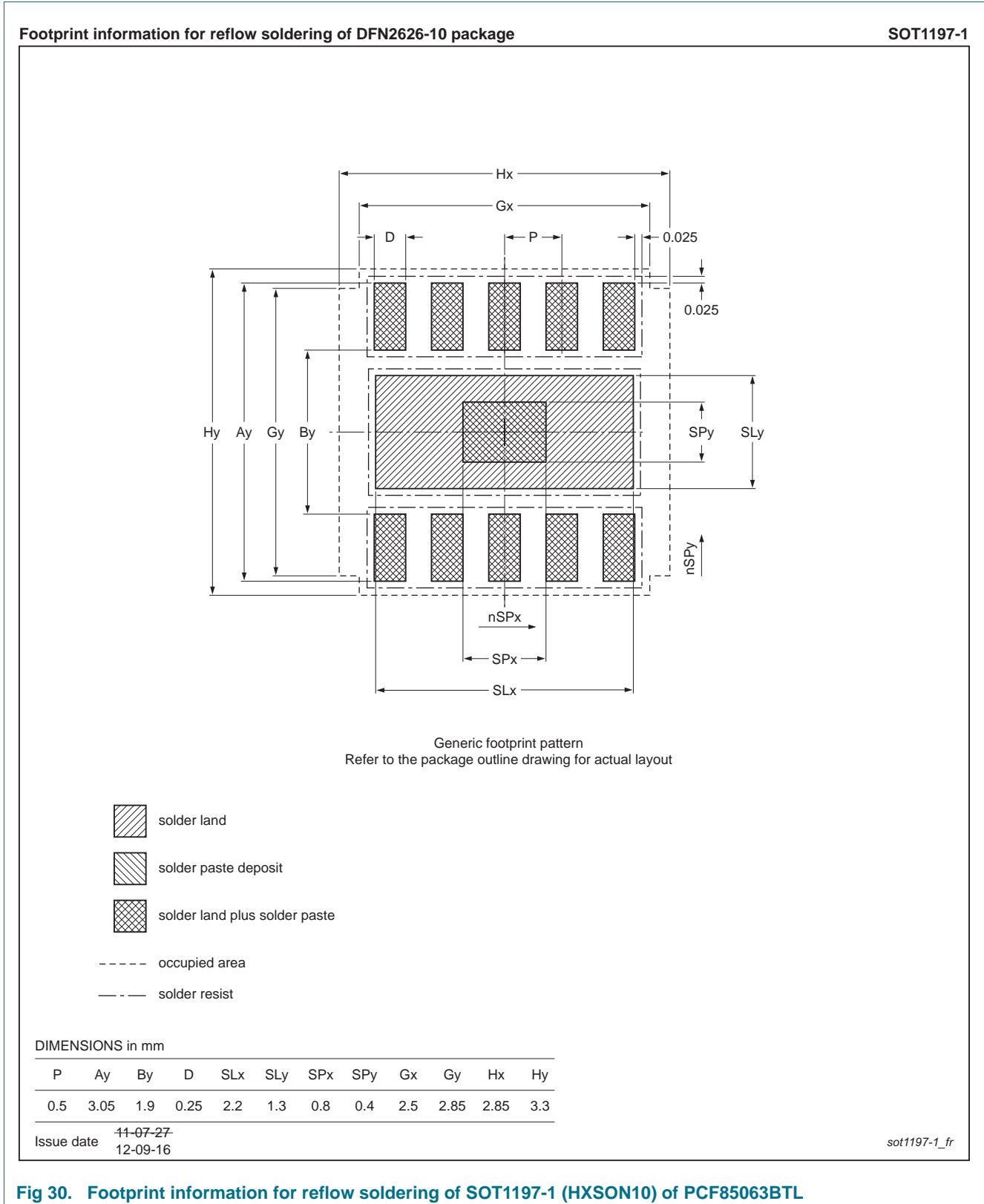


Fig 30. Footprint information for reflow soldering of SOT1197-1 (HXSON10) of PCF85063BTL

19. Abbreviations

Table 47. Abbreviations

| Acronym | Description |
|---------|---|
| AM | Ante Meridiem |
| BCD | Binary Coded Decimal |
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| IC | Integrated Circuit |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| PCB | Printed-Circuit Board |
| PM | Post Meridiem |
| POR | Power-On Reset |
| RAM | Random Access Memory |
| RTC | Real-Time Clock |
| SMD | Surface Mount Device |
| SPI | Serial Peripheral Interface |

20. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10366** — HVQFN application information
- [3] **AN11247** — Improved timekeeping accuracy with PCF85063, PCF8523 and PCF2123 using an external temperature sensor
- [4] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [5] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [6] **IPC/JEDEC J-STD-020** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [7] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [8] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [9] **JESD78** — IC Latch-Up Test
- [10] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [11] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [12] **UM10569** — Store and transport requirements

21. Revision history

Table 48. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|----------------------|---------------|-----------------|
| PCF85063BTL v.2 | 20130415 | Product data sheet | - | PCF85063BTL v.1 |
| Modifications: | <ul style="list-style-type: none"> • Adjusted block diagram (Figure 1) • Improved description of correction pulses (Table 14 and Table 16) • Adjusted Table 34 and Section 8.6.3 • Enhanced application information (Figure 26) • Adjusted I_{DD} and I_{LI} values (Table 42) • Adjusted SPI-bus timing values (Table 43) | | | |
| PCF85063BTL v.1 | 20130123 | Objective data sheet | - | - |

22. Legal information

22.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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